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भाग 12 बाइनरी न्याय अवयव

Indian Standard

GRAPHICAL SYMBOLS FOR DIAGRAMS IN THE FIELD OF ELECTROTECHNOLOGY

PART 12 BINARY LOGIC ELEMENTS

UDC 681·3·042 : 003·62

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Indian Standard

GRAPHICAL SYMBOLS FOR DIAGRAMS IN THE FIELD OF ELECTROTECHNOLOGY

PART 12 BINARY LOGIC ELEMENTS

NATIONAL FOREWORD

This Indian Standard (Part 12) which is identical with IEC Pub 617-12 (1983) 'Graphical symbols for diagrams — Part 12 : Binary logic elements', issued by the International Electrotechnical Commission (IEC) was adopted by the Bureau of Indian Standards on the recommendation of the Basic Standards on Electronics and Telecommunication Sectional Committee (LTD 1) and approval of the Electronics and Telecommunication Division Council.

The text of IEC Standard has been approved as suitable for publication as Indian Standard without deviations. Certain terminology and conventions are, however, not identical with those used in Indian Standards. Attention is specially drawn to the following:

> Wherever the words 'International Standard' appear, referring to this standard, they should be read as 'Indian Standard'.

In the adopted standard (normative) references appear to certain International Standards for which Indian Standards also exist. The corresponding Indian Standards which are to be substituted in their place are listed below along with their degree of equivalence for the editions indicated:

International Standard	*Indian Standard*	*Degree of Correspondence*
IEC Pub 117-15 (1972) Recommended graphical symbols — Part 15 : Binary logic elements	IS 2032 (Part 24) : 1980 Graphical symbols used in electrotechnology: Part 24 Binary logic elements	Technically equivalent
IEC Pub 617-1 (1985) Graphical symbols for diagrams — Part 1 : General information, general index — Cross reference tables	IS 12032 (Part 1) : 1987 Graphical symbols for diagrams in the field of electrotechnology: Part 1 General information	Identical
IEC Pub 617-2 (1983) Graphical symbols for diagrams — Part 2 : Symbol elements, qualifying symbols and other symbols having general applications	IS 12032 (Part 2) : 1987 Graphical symbols for diagrams in the field of electrotechnology : Part 2 Symbol elements, qualifying symbols and other symbols having general applications	Identical
IEC Pub 617-3 (1983) Graphical symbols for diagram — Part 3 : Conductors and connecting devices	IS 12032 (Part 3) : 1987 Graphical symbols for diagrams in the field of electrotechnology : Part 3 Conductors and connecting devices	Identical
IEC Pub 617-10 (1983) Graphical symbols for diagrams — Part 10 : Telecommunications and transmission	IS 12032 (Part 10) : 1990 Graphical symbols for diagrams in the field of electrotechnology : Part 10 Telecommunications and transmission	Identical
IEC Pub 617-13 (1978) Graphical symbols for diagrams — Part 13 : Analogue elements	IS 12032 (Part 13) : 1990 Graphical symbols for diagrams in the field of electrotechnology : Part 13 Analogue elements	Identical

The Basic Standards on Electronics and Telecommunication Sectional Committee has reviewed the provisions of the following IEC Standard and has decided that it is acceptable for use in conjunction with this standard :

IEC Pub 113-7 (1981) Diagrams, charts, tables – Part 7 : Preparation of logic diagrams

This Indian Standard is the twelfth part of the series of Indian Standards on Graphical symbols for diagrams, other parts are :

Part 1 General information
Part 2 Symbol elements, qualifying symbols and other symbols having general application
Part 3 Conductors and connecting devices
Part 4 Passive components
Part 5 Semiconductors and electron tubes
Part 6 Production and conversion of electrical energy
Part 7 Switch gear, control gear and productive devices
Part 8 Measuring instruments, lamps and signalling devices
Part 9 Telecommunication; switching and peripheral equipment
Part 10 Telecommunications; transmission
Part 11 Architectural and topographical installation plans and diagrams
Part 13 Analogue elements

Only the English language text in the International Standard has been retained while adopting it in this Indian Standard.

Indian Standard
GRAPHICAL SYMBOLS FOR DIAGRAMS IN THE FIELD OF ELECTROTECHNOLOGY

PART 12 BINARY LOGIC ELEMENTS

CHAPTER I : GENERAL

SECTION 1 - INTRODUCTION

1.1 This standard contains graphical symbols which have been developed to represent logic functions. They are intended also to represent physical devices capable of carrying out these functions. The symbols have been prepared with a view to electrical applications but the majority may also be applied to non-electrical devices, for example pneumatic, hydraulic, mechancial.

SECTION 2 - GENERAL NOTES

2.1 Symbols in accordance with the superseded IEC Publication 117-15: Recommended Graphical Symbols, Part 15 : Binary Logic Elements, will be required for a prolonged changeover period but should be progressively superseded by the symbols given in this standard. Although non-preferred, the use of other symbols recognized by official national standards, i.e. distinctive shapes in place of symbols 12-27-01, 12-27-02, 12-27-09, 12-27-10, 12-27-11, 12-27-12, 12-28-01, 12-28-02 and 12-28-04, shall not be considered to be in contradiction with this standard. Usage of these other symbols in combination to form complex symbols (e.g. use as embedded symbols) is discouraged.

2.2 For explanation of "logic states", "logic levels", etc., see IEC Publication 113-7: Diagrams, Charts, Tables, Part 7 : Preparation of Logic Diagrams.

2.3 This standard uses the symbols 0 and 1 to identify the two logic states of a binary variable. These states are referred to as 0-state and 1-state.

2.4 A binary variable may be equated to any physical quantity for which two distinct ranges can be defined. In this standard these distinct ranges are referred to as logic levels and are denoted H and L.

H is used to denote the logic level with the more positive algebraic value, and L is used to denote the logic level with the less positive algebraic value.

2.5 In the case of system in which logic states are equated with other qualities of a physical quantity (e.g. positive or negative pulses, presence or absence of a pulse), H and L may be used to represent these qualities or may be replaced by more suitable designations.

SECTION 3 - EXPLANATION OF TERMS

To facilitate understanding of the descriptions in the rest of this standard, it is useful to define three terms.

3.1 "Internal logic state" describes a logic state assumed to exist inside a symbol outline at an input or an output.

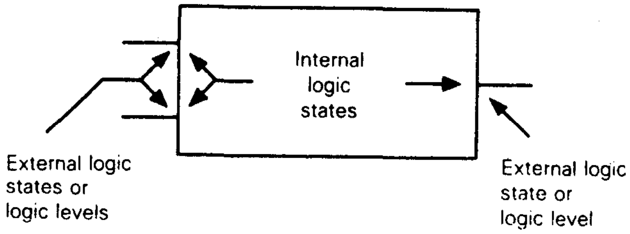
3.2 "External logic state" describes a logic state assumed to exist outside a symbol outline:

- on an input line prior to any external qualifying symbol at that input, or

- on an output line beyond external qualifying symbol at that output.

3.3 "Logic level" describes the physical quality assumed to represent a logic state of a binary variable (see Clauses 2.3 and 2.4).

Illustration

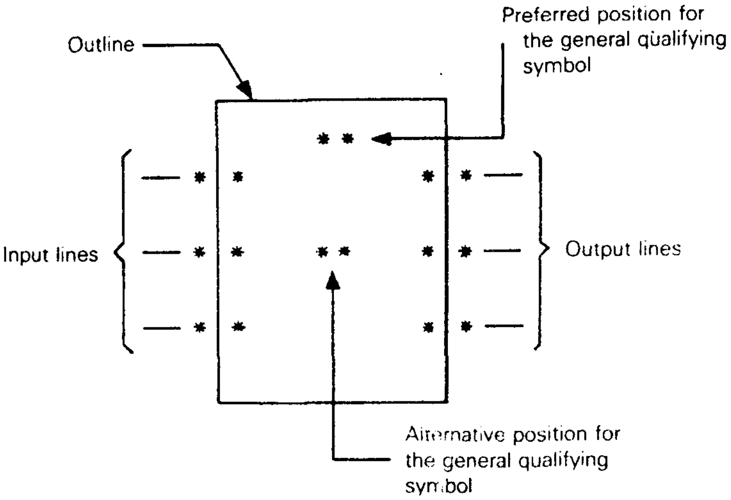


CHAPTER II : SYMBOL CONSTRUCTION

SECTION 4 - COMPOSITION OF THE SYMBOL

4.1 A symbol comprises an outline or combination of outlines together with one or more qualifying symbols.

Application of the symbols requires in addition the representation of input and output lines.


Outline
Preferred position for the general qualifying symbol
Input lines
Output lines
Alternative position for the general qualifying symbol
* *
*

Notes 1. – The single asterisk (*) denotes possible positions for qualifying symbols relating to inputs and outputs.

2. – If and only if the function of an element is completely determined by the qualifying symbols associated with its inputs and/or outputs, no general qualifying symbol is needed.

4.2 General additional information may be included in a symbol outline as described in IEC Publication 113-7: Diagrams, Charts and Tables, Part 7: Preparation of Logic Diagrams.

4.3 Information not standardized in this standard relating to a specific input [output] may be shown in brackets inside the outline adjacent to the relevant input [output] and should follow [precede] any qualifying symbols applying to the input [output] as shown in symbol 12-28-14.

Additional information relating to the general logic function of the element may be shown in brackets inside the outline.

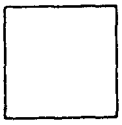
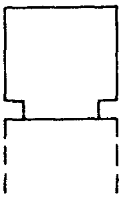
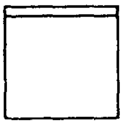
4.4 All outputs of an element represented by a single unsubdivided symbol always have identical internal logic states determined by the function of the element except when indicated otherwise by an associated qualifying symbol or label inside the symbol outline. The subdivision of a symbol and the qualifying symbols referred to here include those explicitly shown and those only implied according to the simplification rules of Clause 6.3.

4.5 In some figures, lower case letters which are not part of the symbols have been shown outside the outline just to identify the inputs and outputs as referenced in the description.

SECTION 5 - OUTLINES

5.1 The length-width ratio of outlines is arbitrary.

5.2 For combinations of outlines, see Section 6.

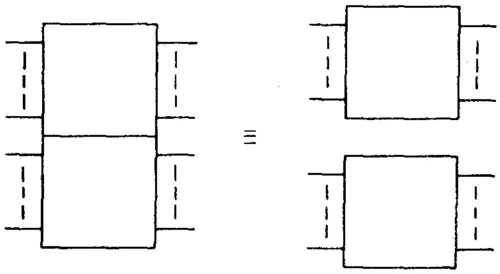
No.	Symbol	Description
12-05-01		Element outline (square shown)
12-05-02		Common control block outline
12-05-03		Common output element outline

SECTION 6 - USE AND COMBINATION OF OUTLINES

6.1 To reduce the space required for the representation of a group of associated elements, the outlines of the elements may be joined or embedded provided the following rules are observed.

6.1.1 There is no logic connection between elements when the line common to their outlines is in the direction of signal flow.

Illustration



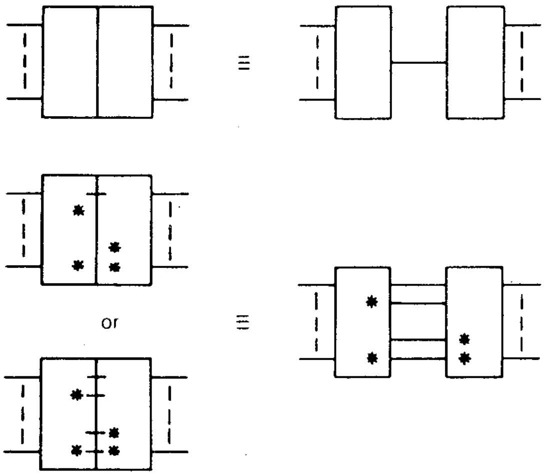
Note. – This rule does not necessarily apply in those arrays in which there exist two or more directions of signal flow, e.g. indicated by a common control block, a common output element, or by dependency notation.

6.1.2 There is at least one logic connection if the line common to two outlines is perpendicular to the direction of signal flow.

Each connection can be shown by the presence of qualifying symbols at one or both sides of the common line. If confusion can arise about the number of logic connections, use can be made of the internal connection symbol (symbol 12-08-01).

If no indications are shown on either side of the common line, it is assumed that there exists only one logic connection.

Illustrations



Each asterisk denotes a position for a qualifying symbol.

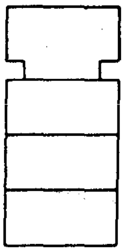
6.2 The common control block may be used in conjunction with an array of related elements as a point of placement for inputs or outputs associated with more than one element of the array, or with no element of the array. Such inputs and outputs shall be labelled if appropriate.

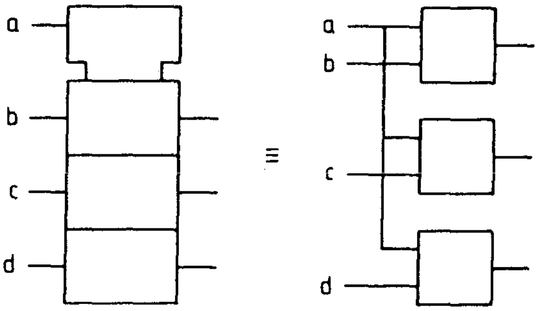
6.2.1 If an input shown at a common control block is an affecting input in the sense of dependency notation (see Sections 11 and 12), it is connected as an input only to those elements of the array in which its identifying number appears. If an input shown at a common control block is not an affecting input in the sense of dependency notation, it is an input common to, or affecting, all elements of the array.

The common control block is placed on one end of an array of related elements.

Unless indicated otherwise, the element next to the common control block is assumed to be the lowest order element.

Illustrations





6.2.2 A common output, depending on all elements of the array, can be shown as the output of a common output element. In the case where any array element has more than one output, the common output element may be used *only* if those outputs always have identical internal logic states. There is one internal connection from each of the elements to the common output element and these shall not be shown. In addition, the common output element may have other inputs and they must be explicitly shown. The function of the common output element shall be indicated.

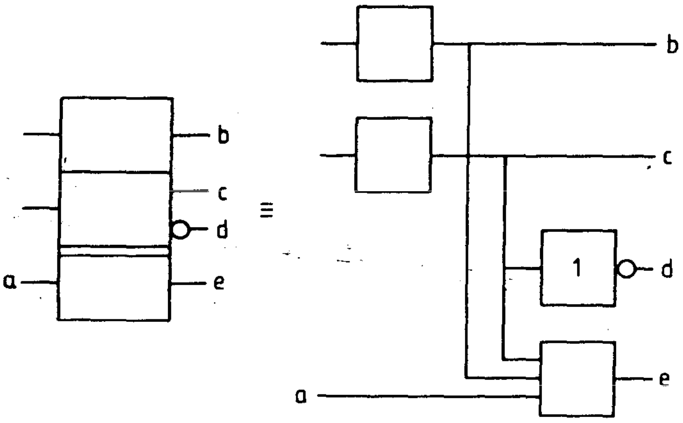
Each input of a common output element corresponding with an output of the array has the same internal logic state as that output.

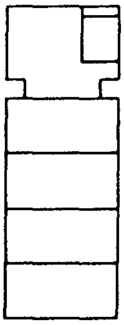
A common output element is shown:

- inside the common control block, or
- at the end of the array, opposite the common control block if there is one.

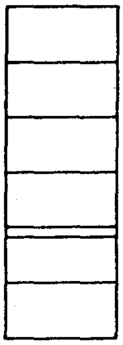
Where it is appropriate to show an array of common output elements, the double line need be shown only once.

Illustrations





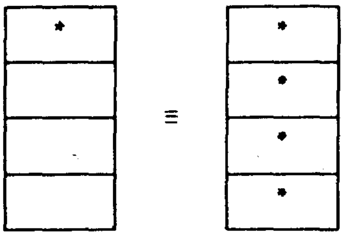
Array with common output element inside the common control block.



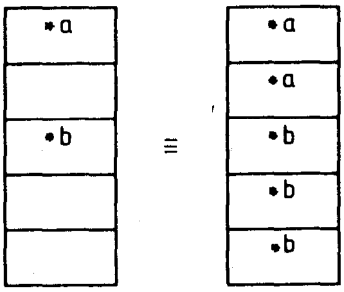
Array with two common output elements

6.3 To represent an array of elements having the same qualifying symbols, it may be sufficient to show the symbols that are inside the outline in only the first of the outlines, provided no confusion can arise. Similarly, in the case of an array of elements each consisting of several identical subarrays, it is sufficient to show the first one in full and to represent each of the others by a simple outline. It is assumed that the identifying numbers of affecting inputs [outputs] in the sense of dependency notation and of inputs [outputs] affected thereby differ in each element of the array (for illustration of the concept see Section 14). See also the simplifications resulting from the use of dependency notation.

Illustrations

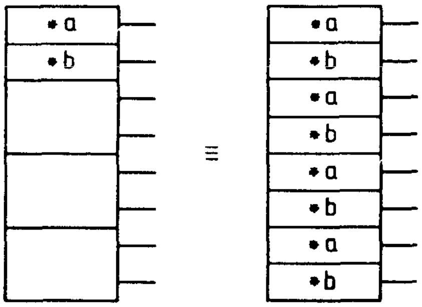


Group of elements with identical general qualifying symbols

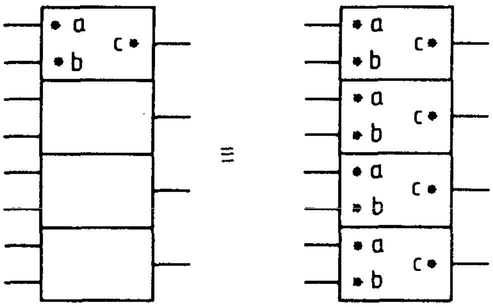


Two successive groups of elements

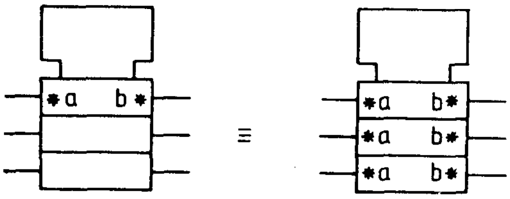
(*Continued overleaf*)



Two interlaced groups of elements



Group of elements with identical qualifying symbols associated with inputs and outputs, shown without common control block



Group of elements with identical qualifying symbols associated with inputs and outputs, shown with common control block

CHAPTER III : QUALIFYING SYMBOLS ASSOCIATED WITH INPUTS, OUTPUTS AND OTHER CONNECTIONS

SECTION 7 – NEGATION, LOGIC POLARITY AND DYNAMIC INPUT

7.1 Each of the symbols in this section defines the relationship between an internal logic state and an external logic state or level.

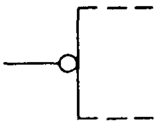
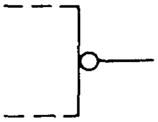
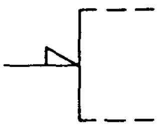
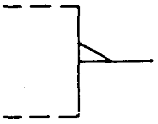
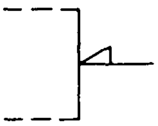
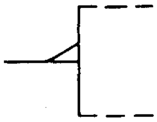
If none of the symbols of this section is shown at an input or output, it is assumed that the internal logic 1-state corresponds with:

- the external logic 1-state in a diagram using the symbol for logic negation, or
- the logic H-level in a diagram using the symbol for logic polarity.

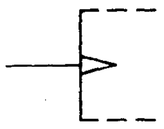
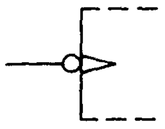
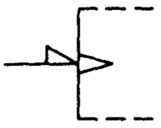
In the latter diagram, external logic states do not exist.

The symbols for logic negation and logic polarity shall not be used together on the same diagram, except when internal connections with logic negation are to be shown on diagrams using the symbol for logic polarity. See symbols 12-08-02 and 12-08-04.

See also IEC Publication 113-7.

No.	Symbol	Description
12-07-01		Logic negation, shown at an input
12-07-02		Logic negation, shown at an output The internal 1-state corresponds with the external 0-state. *Note.* – The connecting line may extend through the circle.
12-07-03		Logic polarity, shown at an input Polarity indicator, shown at an input
12-07-04		Logic polarity, shown at an output Polarity indicator, shown at an output
12-07-05		Logic polarity } shown at an input in the case Ploarity indicator } of signal flow from right to left
12-07-06		Logic polarity } shown at an output in the case Polarity indicator } of signal flow from right to left The internal 1-state corresponds with the L-level on the connecting line.

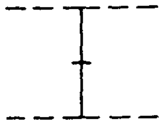
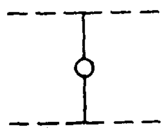
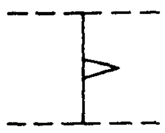
(Continued overleaf)

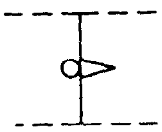
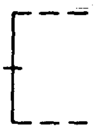
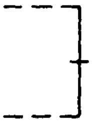
No.	Symbol	Description
12-07-07		**Dynamic input** The (transitory) internal 1-state corresponds with the transition from the external 0-state to the external 1-state. At all other times, the internal logic state is 0. On diagrams using the symbol for logic polarity the (transitory) internal 1-state corresponds with the transition from the L-level to the H-level on the connecting line. At all other times, the internal logic state is 0.
12-07-08		Dynamic input with logic negation The (transitory) internal 1-state corresponds with the transition from the external 1-state to the external 0-state. At all other times the internal logic state is 0.
12-07-09		Dynamic input with polarity indicator The (transitory) internal 1-state corresponds with the transition from the H-level to the L-level on the connecting line. At all other times, the internal logic state is 0.

SECTION 8 – INTERNAL CONNECTIONS

8.1 The symbols in this section define the relationships between internal logic states at internal connections.

An internal connection is a connection within a logic element. It is useful to be able to symbolize such a connection in order to show the logic relationships between elements whose outlines are combined. In many applications, it is also convenient to use the symbols in this section to show the function of complex elements. In such cases, dependency notation should be used to define the effects of any internal inputs or outputs.

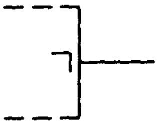
No.	Symbol	Description
12-08-01		Internal connection The internal 1-state [0-state] of the input of the element on the right corresponds with the internal 1-state [0-state] of the output of the element on the left. *Note.* – This symbol may be omitted if no confusion can arise (see also Sub-clause 6.1.2).
12-08-02		Internal connection with negation The internal 1-state [0-state] of the input of the element on the right corresponds with the internal 0-state [1-state] of the output of the element on the left. *Note.* – The vertical line may extend through the circle.
12-08-03		Internal connection with dynamic character The (transitory) internal 1-state of the input of the element on the right corresponds with the transition from the internal 0-state to the internal 1-state of the output of the element on the left. At all other times, the internal logic state of the input of the element on the right is 0.

No.	Symbol	Description
12-08-04		Internal connection with negation and dynamic character The (transitory) internal 1-state of the input of the element on the right corresponds with the transition from the internal 1- state to the internal 0-state of the output of the element on the left. At all other times, the internal logic state of the input of the element on the right is 0.
12-08-05		Internal input (virtual input) This input always stands at its internal 1-state unless it is affected by a dependency relationship that has an overriding or modifying effect (see symbols 12-42-12 and 12-49-02). *Notes 1.* – Internal inputs and outputs have internal logic states only. *2.* – Symbols of Section 7 shall not be applied to internal inputs and outputs, except symbol 12-07-07.
12-08-06		Internal output (virtual output) The effect of this output on an internal input to which it is connected must be indicated by dependency notation. The notes with symbol 12-08-05 apply.

SECTION 9 – SYMBOLS INSIDE THE OUTLINE

9.1 If two or more inputs have the same qualifying symbol for the function, they are assumed to stand in an OR-relation, except in the cases of bi-threshold and extension inputs (see symbols 12-09-02 and 12-09-09) where the relationship should be appropriately indicated.

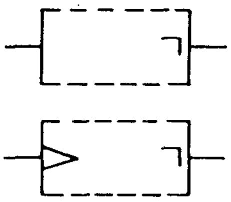
9.2 The descriptions of symbols 12-09-13 to 12-09-22 may give the reader the wrong impression that these are dynamic inputs. This is not the case, as it must be remembered that the internal logic state as determined by the external logic state or level may possibly be modified by the effect of other inputs (e.g. Cm- inputs). If inputs represented by symbols 12-09-13 to 12-09-22 have a dynamic character, symbol 12-07-07 should be used in addition. See for example symbol 12-47-01.

No.	Symbol	Description
12-09-01		Postponed output The change of the internal state of this output is postponed until the input signal which initiates the change returns to its initial external logic state or logic level. The internal logic state of any input(s) affecting or affected by the initiating input must not change while this initiating input stands at its internal 1-state or the resulting output state will not be specified by the symbol. If the input signal which initiates the change appears at an internal connection, the change of state is postponed until the output of the preceding element returns to its initial internal logic state. *Notes 1.* – If this symbol is shown without prefix, it should be assumed that the output is postponed with respect to *each* →, ←, +, –. T-input and to *each* Cm-input, or Cm-output (see symbols 12-18-01 and 12-18-02); in all other cases, the identifying numbers (or if necessary the full labels) of all inputs and outputs with respect to which the output is postponed must be shown as a prefix to this symbol. See symbol 12-19-15. *2.* – Care should be taken that this symbol is a right angle with lines of equal length to avoid confusion with other symbols, for example the character 7. *3.* – For the application of this symbol and additional explanation, see Section 41.

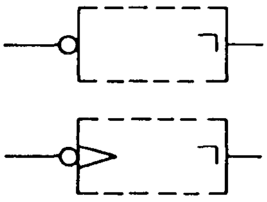
Illustrations

If there are no other inputs with an overriding effect, the transition at the output takes place when the input changes

- in a diagram using the symbol for logic negation:

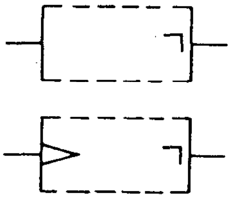


from its external 1-state to its external 0-state

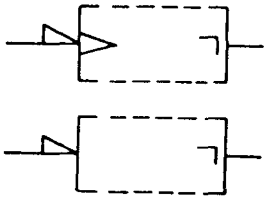


from its external 0-state to its external 1-state

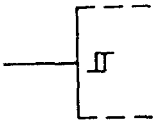
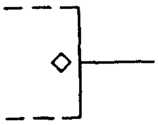
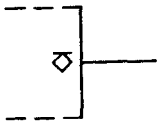
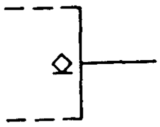
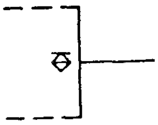
- in a diagram using the symbol for logique polarity:



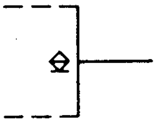
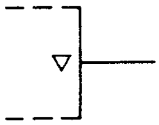
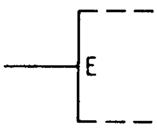
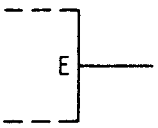
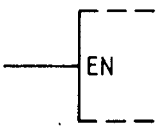
from its H-level to its L-level



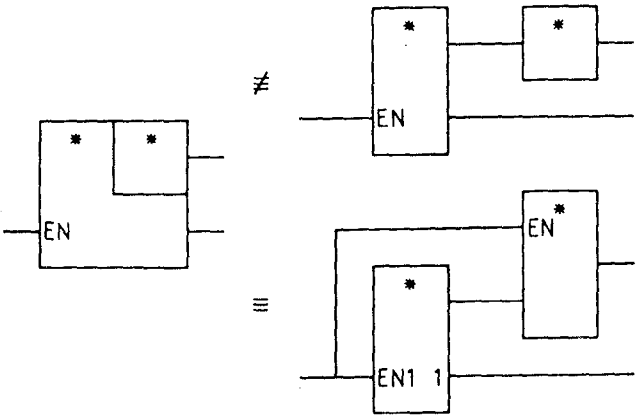
from its L-level to its H-level

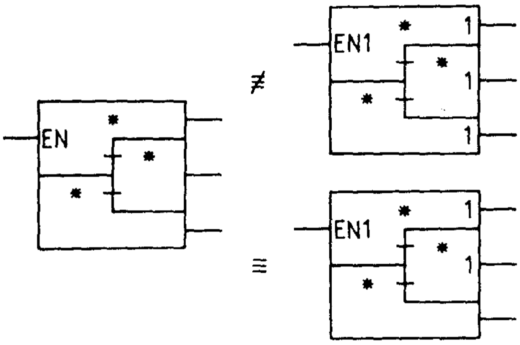
No	Symbol	Description
12-09-02		Bi-threshold input Input with hysteresis The input takes on its internal 1-state when the external signal level reaches a threshold value V1. It maintains this state until the external signal level has returned through V1 and reaches another threshold value V2. If this symbol (without the negation symbol or polarity symbol) appears on a diagram that uses either the symbol for logic polarity or the positive-logic convention, V1 is more positive than V2. If it appears on a diagram that uses the negative-logic convention, V1 is more negative than V2. If the negation or polarity symbol is present at the input, then the relationship between V1 and V2 is reversed. *Note.* – If the label at the input line includes other symbols, symbol 12-09-02 shall be drawn adjacent to the input line.
12-09-03		Open-circuit output (e.g. open-collector, open-emitter, open-drain, open-source) One of the two possible internal logic states of this type of output corresponds with an external high-impedance condition. In order to produce a proper logic level in this condition, an externally connected component or circuit, often a resistor, is required. This type of output is usually capable of forming part of a distributed connection. *Notes 1.* – This symbol shall be drawn adjacent to the output line, except when using the bit-grouping symbol (symbol 12-09-25) in the manner defined in Section 25, where an alternative position is permitted. *2.* – Although this symbol is shown inside the outline, it refers to external states and levels only. *3.* – If it is necessary to indicate which logic level is the one with the low impedance, use can be made of symbol 12-09-04 or 12-09-05.
12-09-04		Open-circuit output (H-type), for example PNP open-collector, NPN open-emitter, P-channel "open-drain", N-channel "open-source". When not in its external high-impedance condition, this type of output produces a relatively low-impedance H-level. See also symbol 12-27-13. Notes 1 and 2 with symbol 12-09-03 apply. *Note.* – The meaning of this symbol is not altered by the presence of a negation or polarity indicator.
12.-09-05		Open-circuit output (L-type), for example NPN open-collector, PNP open-emitter, N-channel "open-drain", P-channel "open-source". When not in its external high-impedance condition this type of output produces a relatively low-impedance L-level. See also symbol 12-27-13. Notes 1 and 2 with symbol 12-09-03 and the note with symbol 12- 09-04 apply.
12-09-06		Passive-pull-down output This type of output is similar to H-type open-circuit output (symbol 12-09-04) and can likewise be used as part of a distributed connection but without the need for an additional external component or circuit. See also symbol 12-27-13. Note 1 with symbol 12-09-03 and the note with symbol 12-09-04 apply.

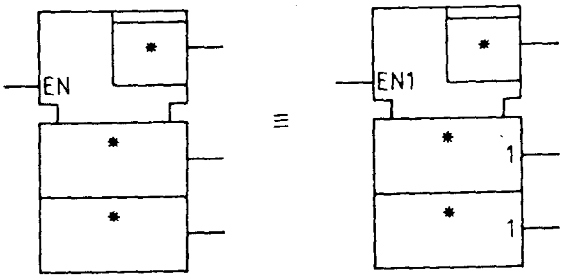
(Continued overleaf)

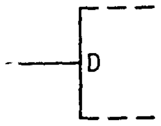
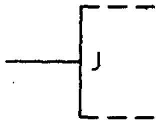
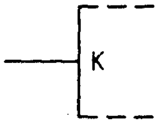
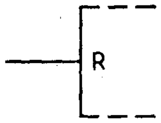
No.	Symbol	Description
12-09-07		Passive-pull-up output This type of output is similar to the H type open circuit output (symbol 12-09-05) and can likewise be used as part of a distributed connection but without the need for an additional external component or circuit. See also symbol 12-27-13. Note 1 with symbol 12-09-03 and the note with symbol 12-09-04 apply
12-09-08		3-state output This output can take on a third external state, which is a high-impedance condition, having no logic significance. For an example of use, see symbol 12-29-04. Note 1 with symbol 12-09-03 applies.
12-09-09		Extension input An input of a binary element to which the output of an extender element may be connected (see symbol 12-09-10). *Note.* – The description which characterizes the relationship between the external logic states of binary variables and their corresponding physical quantities is normally not valid for extension inputs and extender outputs.
12-09-10		Extender output An output of a binary element which may be connected to the extension input of another binary element in order to extend the number of inputs of that element. The note with symbol 12-09-09 applies.
12-09-11		Enable input If this input stands at its internal 1-state, all outputs stand at their normally defined internal logic states and have their normally defined effect on elements or distributed connections that may be connected to the outputs, provided no other inputs or outputs have an overriding and contradicting effect. If the input stands at its internal 0-state, all outputs of the type 12-09-03, 12-09-04 or 12-09-05 are in their external high-impedance conditions, all passive-pulldown outputs stand at their high-impedance L-levels, all passive-pull-up outputs stand at their high-impedance H-levels, all 3-state outputs stand at their normally defined internal logic states and are in their external high-impedance conditions and all other outputs stand at their internal 0-states. *Note.* – This input only affects outputs shown as external outputs. If it is an input of an element having an internal connection indicated by one of the symbols 12-08-01 to 12-08-04, even-when the note to symbol 12-08-01 is applied, the input is also an EN-input of the element to which the internal connection is connected. If ambiguity can arise, for example in the case of embedded outlines, EN-dependency as defined in Section 20 should be used.

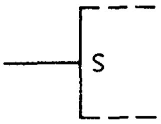
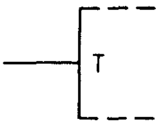
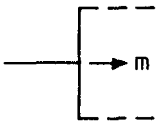
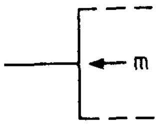
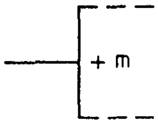
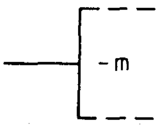
Illustrations

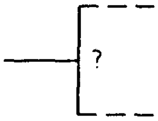
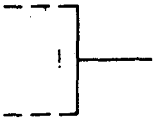
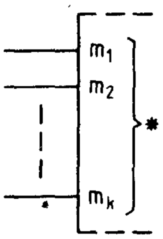
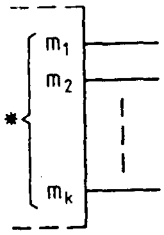




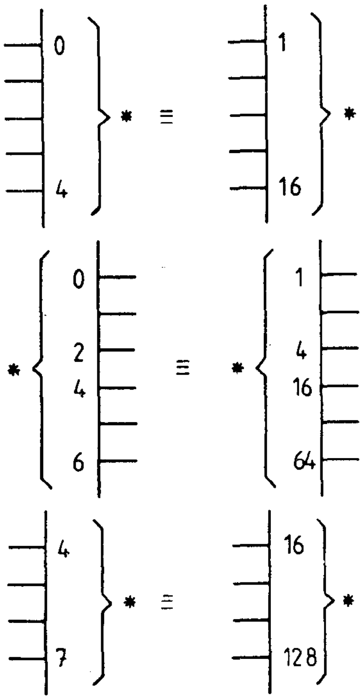


No.	Symbol	Description
12-09-12		D-input The internal logic state of D-input is stored by the element. See symbol 12-42-02. *Note.* – The internal logic state of this input is always subject to an affecting input or output.
12-09-13		J-input When this input takes on its internal 1-state, a1 is stored by the element. When the input stands at its internal 0-state, it has no effect on the element.
12-09-14		K-input When this input takes on its internal 1-state, a 0 is stored by the element. When the input stands at its internal 0-state, it has no effect on the element. Each occurrence of the combination J = K = 1 causes a single change of the internal state of the output to its complement. Clause 9.2 applies.
12-09-15		R-input When this input takes on its internal 1-state, a 0 is stored by the element. When the input stands at its internal 0-state, it has no effect on the element.

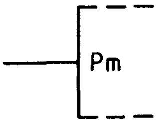
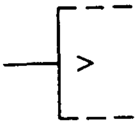
No.	Symbol	Description
12-09-16		S-input When this input takes on its internal 1-state, a 1 is stored by the element. When the input stands at its internal 0-state, it has no effect on the element. The effect of the combination R = S = 1 is not specified by the symbol; this effect may be indicated by means of SET/RESET-dependency (see Section 19). Clause 9.2 applies.
12-09-17		T-input Each time this input takes on its internal 1-state, a single change of the internal state of the output to its complement takes place. When the input stands at its internal 0-state, it has no effect on the element. Clause 9.2 applies.
12-09-18		Shifting input, left to right or top to bottom Each time this input takes on its internal 1-state, the information contained in the element will be shifted once m positions from left to right or from top to bottom, depending on the orientation of the symbol for the element. When the input stands at its internal 0-state, it has no effect on the element. Clause 9.2 applies. *Note.* – m shall be replaced by the relevent value. If m = 1, the 1 may be omitted.
12-09-19		Shifting input, right to left or bottom to top Each time this input takes on its internal 1-state, the information contained in the element will be shifted once m positions from right to left or from bottom to top, depending on the orientation of the symbol for the element. When the input stands at its internal 0-state, it has no effect on the element. Clause 9.2 applies. The note with symbol 12-09-18 applies.
12-09-20		Counting up input Each time this input takes on its internal 1-state, the count of the element is increased once by m units. When the input stands at its internal 0-state, it has no effect on the element. Clause 9.2 applies. The note with symbol 12-09-18 applies.
12-09-21		Counting-down input Each time this input takes on its internal 1-state, the count of the element is decreased once by m units. When the input stands at its internal 0-state, it has no effect on the element. Clause 9.2 applies. The note with symbol 12-09-18 applies.

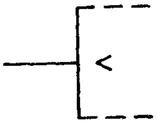
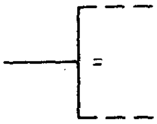
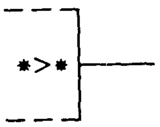
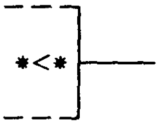
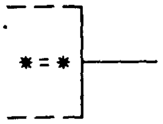
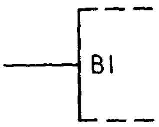
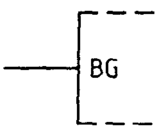
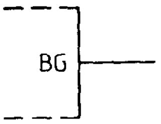
No.	Symbol	Description
12-09-22		Query input of an associative memory Interrogate input of an associative memory If this input takes on its internal 1-state, an interrogation of the content of the element takes place. If the input stands at its internal 0-state, it has no effect on the element. Clause 9.2 applies.
12-09-23		Compare output of an associative memory Match output of an associative memory. The internal 1-state at this output indicates a match.
12-09-24		Bit grouping for multibit input, general symbol Inputs grouped by this symbol produce a number that is the sum of the individual weights of the inputs standing at their internal 1-states. The individual inputs shall be shown in ascending or descending order by weight. This number can be regarded: – as a number on which a mathematical function is performed, or – as defining an identifying number in the sense of dependency notation (according to Clause 24.2), or – as a value to become the content of the element. m_1 ..... m_k shall be replaced by the decimal equivalents of the actual weights. If all weights are powers of 2, m_1 ..... m_k may be replaced by the exponents of the powers of 2. Lables between m_1 and m_k may be omitted to the extent that no confusion can arise. The asterisk must be replaced by an appropriate indication of the operand on which the mathematical function is performed (e.g. P or Q), by an appropriate indication in the sense of dependency notation or by CT. In the latter case, the number produced by the inputs is the value that is loaded into the element.
12-09-25		Bit grouping for multibit output, general symbol Outputs grouped by this symbol represent a number that is the sum of the individual weights of the outputs standing at their internal 1-states. The individual outputs shall be shown in ascending or descending order by weight. This number can be regarded: – as the result of the performance of a mathematical function, or – as the value of the content of the element. m_1 ..... m_k shall be replaced by the decimal equivalents of the actual weights. If all weights are powers of 2, m_1 ...... m_k may be replaced by the exponents of the powers of 2. Labels between m_1 and m_k may be omitted to the extent that no confusion can arise. The asterisk must be replaced by an appropriate indication of the result of the performance of the mathematical function or by CT. In the latter case, the number represented by the outputs standing at their internal 1-states is the actual value of the content of the element.

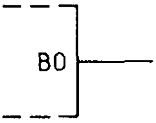
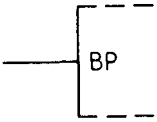
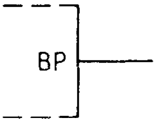
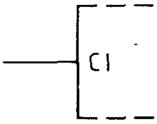
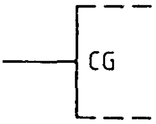
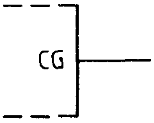
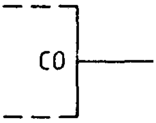
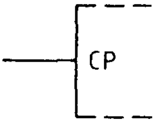
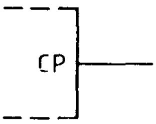
Illustrations

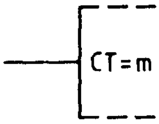
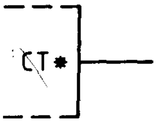
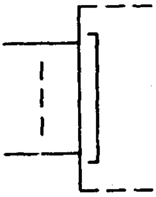
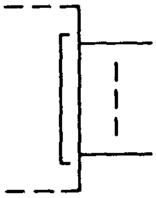
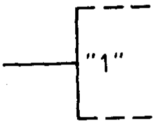
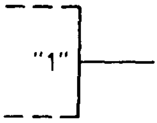


See also examples in Section 39

No.	Symbol	Description
12-09-26		Operand input (Pm-input shown) This input represents one bit of an operand on which one or more mathematical functions are performed. *Notes 1.* - m shall be replaced by the decimal equivalent of the weight of the bit. If the weights of all Pm-inputs of the element are powers of 2, at each Pm-input m may be replaced by the exponent of the power of 2. *2.* - If an operand consists of two or more bits represented by adjacent input lines, the bit grouping symbol (12-09-24) may be used. *3.* - Preferred letters for operands are P and Q. If these letters are not suitable or if more than two operands are involved, other characters may be used providing no confusion can arise.
12-09-27		Greater-than input of a magnitude comparator *Notes 1.*— This symbol is intended for use when representing cascaded comparators. For an example of use, see symbol 12-39- 08. *2.* - Symbols 12-09-27, 12-09-28 and 12-09-29 may be combined to qualify inputs as follows: ≥, ≤, ≷. *3.* - This symbol should not be drawn adjacent to the outline, to avoid confusion with the dynamic input indicator symbol (12-07-07).

No.	Symbol	Description
12-09-28		Less-than input of a magnitude comparator Notes 1 and 2 with symbol 12-09-27 apply.
12-09-29		Equal input of a magnitude comparator Notes 1 and 2 with symbol 12-09-27 apply.
12-09-30		Greater-than output of a magnitude comparator *Notes 1.* – The asterisks shall be replaced by designations of the operands, for example P and Q respectively. 2. – Symbols 12-09-30, 12-09-31 and 12-09-32 may be combined to qualify outputs as follows: $* \geq *$, $* \leq *$, $\gtrless$. 3. – If this symbol appears in one element of a series of cascaded comparators, the output marked with this symbol is affected not only by the operands, but also by the inputs marked with the symbols 12-09-27, 12-09-28 or 12-09-29.
12-09-31		Less-than output of a magnitude comparator The notes with symbol 12-09-30 apply.
12-09-32		Equal output of a magnitude comparator The notes with symbol 12-09-30 apply. *Note.* – If this symbol is not combined with symbol 12-09-30 or symbol 12-09-31, the designations of the operands may be omitted providing no confusion can arise.
12-09-33		Borrow-in input of an arithmetic element *Note.* – A number may be added as a suffix to this label; this number is the exponent of the power of 2 which is the weight of the bit involved.
12-09-34		Borrow-generate input of an arithmetic element The note with symbol 12-09-33 applies.
12-09-35		Borrow-generate output of an arithmetic element The note with symbol 12-09-33 applies.

No.	Symbol	Description
12-09-36		Borrow-out output of an arithmetic element Ripple-borrow output of an arithmetic element The note with symbol 12-09-33 applies.
12-09-37		Borrow-propagate input of an arithmetic element The note with symbol 12-09-33 applies.
12-09-38		Borrow-propagate output of an arithmetic element The note with symbol 12-09-33 applies.
12-09-39		Carry-in input of an arithmetic element The note with symbol 12-09-33 applies.
12-09-40		Carry-generate input of an arithmetic element The note with symbol 12-09-33 applies.
12-09-41		Carry-generate output of an arithmetic element The note with symbol 12-09-33 applies.
12-09-42		Carry-out output of an arithmetic element Ripple-carry output of an arithmetic element The note with symbol 12-09-33 applies.
12-09-43		Carry-propagate input of an arithmetic element The note with symbol 12-09-33 applies.
12-09-44		Carry-propagate output of an arithmetic element The note with symbol 12-09-33 applies.

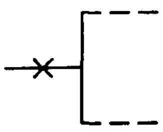
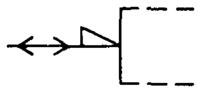
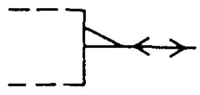
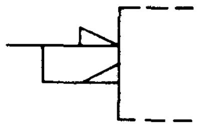
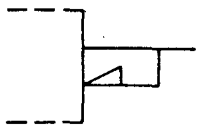
No.	Symbol	Description
12-09-45		Content input m shall be replaced by an appropriate indication of the content of the element (e.g. a counter) that results whenever this input takes on its internal 1-state. If this input stands at its internal 0-state, it has no effect on the element. For an example of use, see symbol 12-49-16.
12-09-46		Content output The asterisk shall be replaced by an appropriate indication of those values of the content of the element (e.g. a counter) for which the output stands at its internal 1-state. For an example of use, see symbol 12-49-12.
12-09-47		Line grouping at the input side This symbol indicates that two or more connections are needed to implement a single logic input. For an example of use, see symbol 12-28-06. *Notes. 1.* - The logic levels on connections grouped by this symbol may differ from those on the other input and output pins. *2.* - For an example of use of Note 1, see symbol 12-29-07.
12-09-48		Line grouping at the output side This symbol indicates that two or more connections are needed to implement a single logic output. For an example of use, see symbol 12-28-07. Note 1 with symbol 12-09-47 applies.
12-09-49		Fixed-mode input If an element can perform several functions but only a restricted number of functions is of interest, this representation can be used to identify an input that must be in the internal 1-state for the element to perform the functions of interest indicated by the symbol. A fixed mode input must not be affected by dependency notation nor have other functions. For examples of use, see symbols 12-49-07 and 12-49-08.
12-09-50		Fixed state output This representation may be used to identify an output that always stands at its internal 1-state. A fixed-state output must not be affected by dependency notation nor have other functions. For an example of use, see symbol 12-33-10.

SECTION 10 – NON-LOGIC CONNECTIONS AND SIGNAL-FLOW INDICATORS

10.1 Symbol 13-02-01 or 13-02-02 of IEC Publication 617-13 may be used to denote an input or an output carrying analogue or digital signals respectively.

10.2 For supply voltage inputs having special effects, use symbol 13-03-11 of IEC Publication 617-13.

10.3 In principle, the direction of signal flow is from left to right and from top to bottom. If this rule cannot be maintained or the direction of signal flow is not obvious, then the signal lines should be marked with arrowheads pointing in the direction of signal flow. These arrowheads shall not touch the outline or any qualifying symbol. See for example, symbol 12-29-03.

No.	Symbol	Description
12-10-01		Non-logic connection, shown on the left-hand side This symbol may be used to indicate a connection which does not carry any logic information (e.g. reference voltage connection). *Note.* – Additional information associated with non-logic connections may be shown without brackets inside the outline. For an example of use, see symbol 12-47-02.
12-10-02	Use symbol 02-05-03	Bidirectional signal flow For an example of use, see symbol 12-29-08. *Notes. 1.* – On a connecting line with bidirectional signal flow, any symbol for logic polarity should point to the right or down e.g.:  and  *2.* – In some cases, the appearance of the symbols for logic polarity makes the use of the symbol of bidirectional signal flow unnecessary, e.g.:  and 

CHAPTER IV : DEPENDENCY NOTATION

SECTION 11 - GENERAL EXPLANATION

Dependency notation is a means of denoting the relationships between inputs, outputs, or inputs and outputs, without actually showing all the elements and interconnections involved.

Apart from its use in complex elements, dependency notation should not be used to replace the symbols for combinative elements.

The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for dependency notation, use will be made of the terms "affecting" and "affected". In the case where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g. if they stand in an AND relationship), the choice may be made in any convenient way.

In some complex elements, outputs may have an effect on inputs and other outputs. For the sake of simplicity, the text of Sections 12 and 13 refers to "affecting inputs" only, but it should be understood that the recommended notation applies to affecting outputs also.

SECTION 12 - CONVENTION

Dependency notation usually defines relationships between internal logic states. However, in the case of 3-state outputs, passive-pull-down outputs, passive-pull-up outputs, and open-circuit outputs (symbols 12-09-03 through 12-09-08), ENABLE dependency (section 20) defines relationships between the internal logic states of affecting inputs and the external states of affected outputs.

Application of dependency notation is accomplished by:

- labelling the input affecting other inputs or outputs with a particular letter symbol denoting the relationship involved followed by an identifying number;
- labelling each input or output affected by that affecting input with that same number.

If it is the complement of the internal logic state of the affecting input [output] that does the affecting, a bar shall be placed over the indentifying number at the affected input [output]. For an example of use, see symbol 12-42-11.

If the affected input or output requires a label to denote an effect it has on the element, this label shall be prefixed by the identifying number of the affecting input.

If an input or output is affected by more than one affecting input the identifying numbers of each of the affecting inputs shall appear in label of the affected one, separated by commas. The left-to-right order of these identifying numbers is the same as the sequence of the affecting relationships (see also Section 25).

Two affecting inputs labelled with different letters shall not have the same identifying number unless one of the letters is A (see Section 23).

If two affecting inputs have the same letter and the same identifying number they stand in an OR relationship to each other.

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g. outputs of a coder), the identyfying numbers to be associated with both affecting inputs and affected inputs or outputs shall be replaced by another character selected to avoid ambiguity, for example Greek letters.

An affecting input affects only the corresponding affected inputs and outputs of the symbol.

SECTION 13 - TYPES OF DEPENDENCY

13.1 The following types of dependency are defined:

AND, OR and NEGATE dependencies are used to denote Boolean relationships between inputs and/or outputs.

INTERCONNECTION dependency is used to indicate that an input or output imposes it logic state on one or more other inputs and/or outputs.

CONTROL dependency is used to identify a timing input or a clock input of a sequential element and to indicate which inputs are controlled by it.

SET and RESET dependencies are used to specify the internal logic states of an RS-bistable element when the R-and S-inputs both stand at their internal 1-states.

ENABLE dependency is used to identify an Enable input and to indicate which inputs and/or outputs are controlled by it (e.g. which outputs take on their high-impedance condition).

MODE dependency is used to identify an input which selects the mode of operation of an element and to indicate the inputs and/or outputs depending on that mode.

ADDRESS dependency is used to identify the Address inputs of a memory.

Table 1 page 51, lists the various dependencies and summarizes their effects. More detailed definitions appear in the following sections, together with illustrations of the concepts. In these illustrations, general symbols explained in Chapter V are used.

In Table 1, the word "action" implies:

- that affecting inputs will have their normally defined effect on the function of the element;
- that affected outputs will take on the internal logic states determeined by the function of the element.

TABLE I

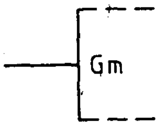
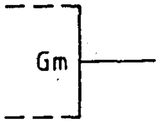
Types of dependency

Type of dependency	Letter(s)	Effect on affected input or output if the affecting input stands at its:		See Section
		1-state	0-state	
ADDRESS	A	Permits action (address selected)	Prevents action (address not selected)	23
CONTROL	C	Permits action	Prevents action	18
ENABLE	EN	Permits action	– Prevents action of affected inputs – Imposes external high-impedance condition on open-circuit and 3-state outputs (internal state of 3-state outputs unaffected) – imposes high-impedance L-level on passive-pull-down outputs and high-impedance H-level on passive-pull-up outputs – Imposes 0-state on other outputs	20
AND	G	Permits action	Imposes 0-state	14
MODE	M	Permits action (mode selected)	Prevents action (mode not selected)	21
NEGATE	N	Complements state	No effect	16
RESET	R	Affected output reacts as it would do to S = 0, R = 1.	No effect	19
SET	S	Affected output reacts as it would do to S = 1, R = 0	No effect	19
OR	V	Imposes 1-state	Permits action	15
INTER CONNECTION	Z	Imposes 1-state	Imposes 0-state	17

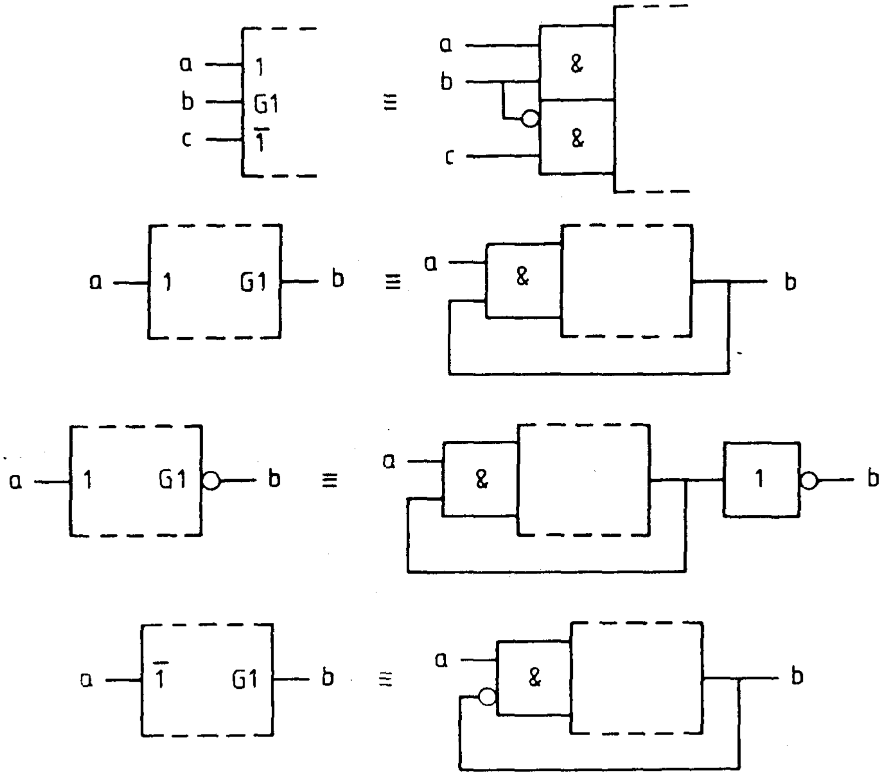
Note. – An affected input [output] carrying an identifying number with a bar over it is affected by the logic state of the affecting input which is the complement of that indicated in the table above.

SECTION 14 – AND DEPENDENCY (G-DEPENDENCY)

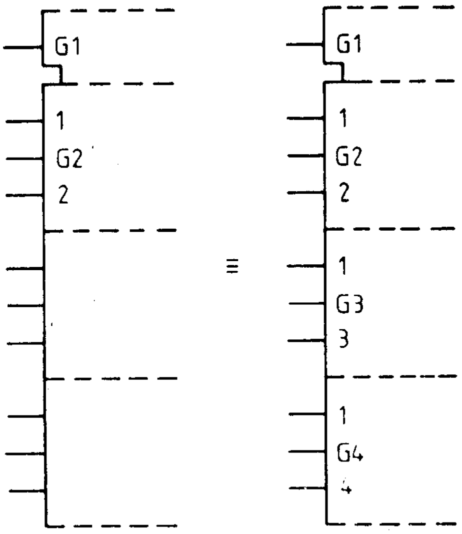
14.1 Each input or output affected by a Gm-input or Gm-output stands in an AND relationship with this Gm-input or Gm-output.

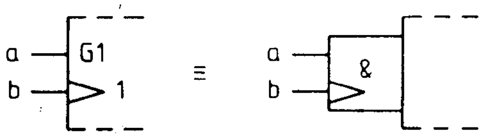
No.	Symbol	Description
12-14-01		Gm-input
12-14-02		Gm-output If a Gm-input or Gm-output stands at its internal 1-state, all inputs and outputs affected by this Gm-input or Gm-output stand at their normally defined internal logic states. If a Gm-input or Gm-output stands at its internal 0-state, all inputs and outputs affected by this Gm-input or Gm-output stand at their internal 0-states. The note with Table 1 applies. *Note.* – m must be replaced by the relevant identifying number.

Illustrations

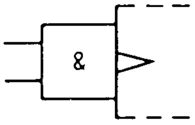


(*Continued overleaf*)



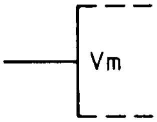
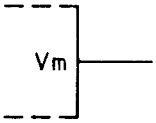


Dependency notation does not provide a shorthand notation for:

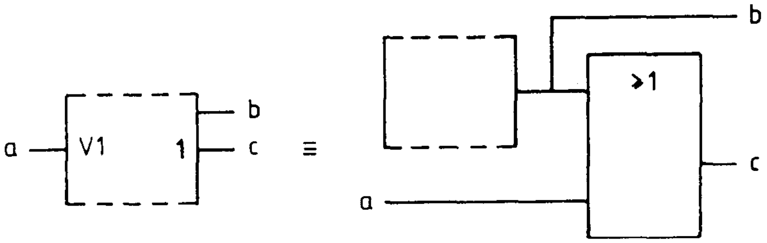


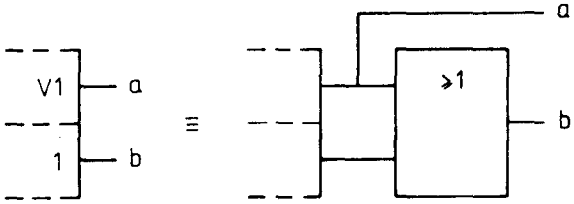
SECTION 15 – OR DEPENDENCY (V-DEPENDENCY)

15.1 Each input or output affected by a Vm-input or Vm-output stands in an OR relationship with this Vm-input or Vm-output.

No.	Symbol	Description
12-15-01		Vm-input
12-15-02		Vm-output
		If a Vm-input or Vm-output stands at its internal 1-state, all inputs and outputs affected by this Vm-input or Vm-output stand at their internal 1-states. If a Vm-input or Vm-output stands at its internal 0-state, all inputs and outputs affected by this Vm-input or Vm-output stand at their normally defined internal logic states. The notes with Table 1 and symbols 12-14-01 and 12-14-02 apply.

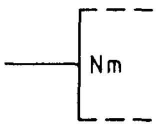
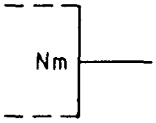
Illustrations



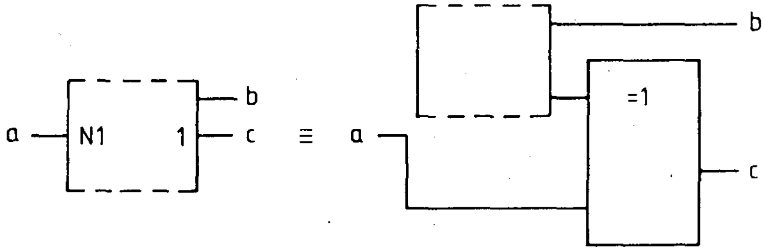


SECTION 16 – NEGATE DEPENDENCY (N-DEPENDENCY)

16.1 Each input or output affected by an Nm-input or Nm-output stands in an EXCLUSIVE-OR relationship with this Nm-input or Nm-output.

No.	Symbol	Description
12-16-01		Nm-input
12-16-02		Nm-output
		If an Nm-input or Nm-output stands at its internal 1-state, the internal logic state of each input and each output affected by this Nm-input or Nm-output is the complement of the normally defined internal logic state of that input or output. If an Nm-input or Nm-output stands at its internal 0-state, all inputs and outputs affected by this Nm-input or Nm-output stand at their normally defined internal logic states. The notes with Table 1 and symbols 12-14-01 and 12-14-02 apply.

Illustration



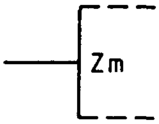
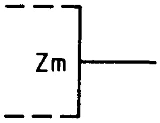
If a = 0, then c = b

If a = 1, then c = $\overline{b}$

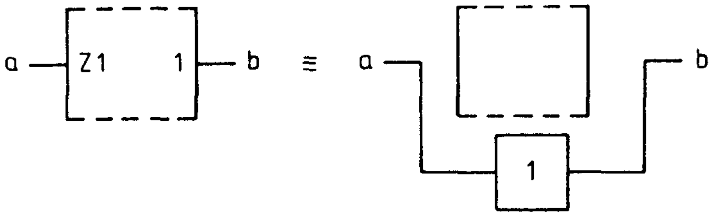
SECTION 17 – INTERCONNECTION DEPENDENCY (Z-DEPENDENCY)

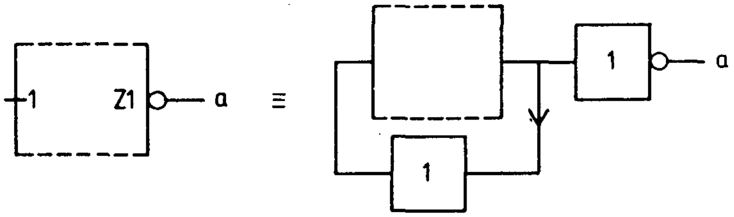
17.1 INTERCONNECTION dependency is used to indicate that an input or output imposes its internal logic state on one or more other inputs and/or outputs, for an example of use, see symbol 12-28-13.

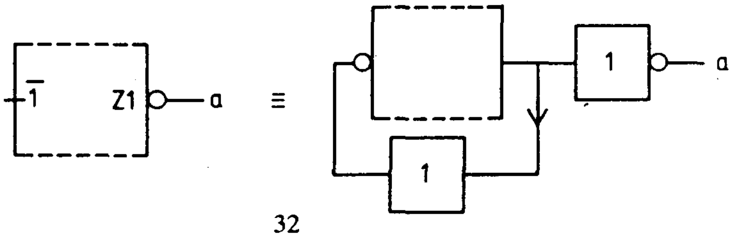
The internal logic state of an input or output affected by a Zm-input or Zm-output is identical to the internal logic state of its affecting Zm-input or Zm-output unless modified by additional dependency notation.

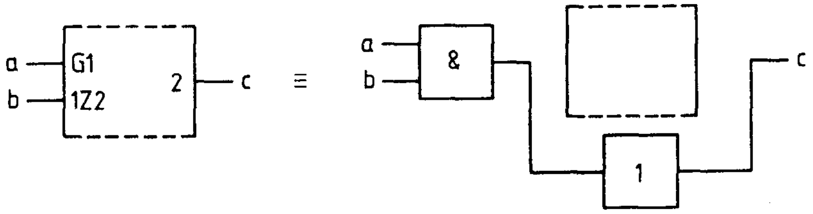
No.	Symbol	Description
12-17-01		Zm-input
12-17-02		Zm-output If a Zm-input or Zm-output stands at its internal 1-state, all inputs and outputs affected by this Zm-input or Zm-output stand at their internal 1-states unless modified by additional dependency notation. If a Zm-input or Zm-output stands at its internal 0-state, all inputs and outputs affected by this Zm-input or Zm-output stand at their internal 0-states unless modified by additional dependency notation. The notes with Table I and symbols 12-14-01 and 12-14-02 apply.

Illustrations



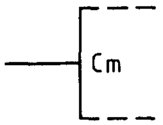
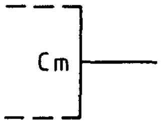




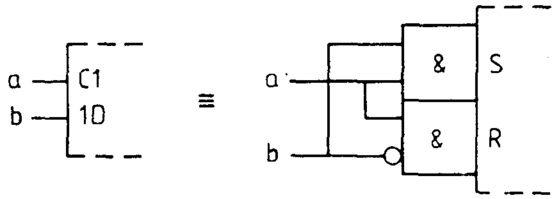


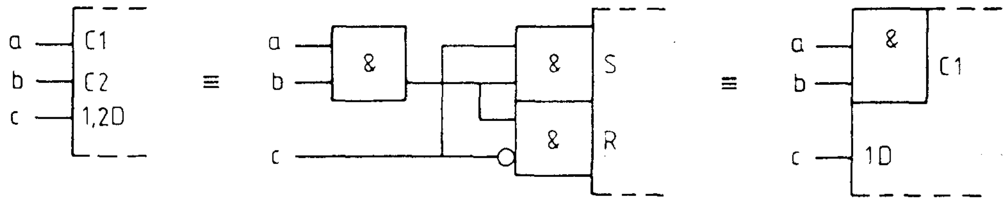
SECTION 18 - CONTROL DEPENDENCY (C-DEPENDENCY)

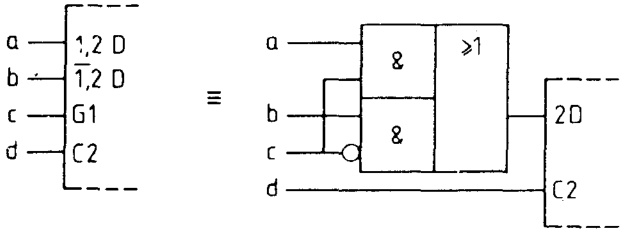
18.1 CONTROL dependency shall be used for sequential elements only and may imply more than a simple AND relationship. It identifies an input that produces action, for example the clock of an edge-triggered bistable circuit or the data enable of a level-operated transparent latch.

No.	Symbol	Description
12-18-01		Cm-input
12-18-02		Cm-output If a Cm-input or Cm-output stands at its internal 1-state, the inputs affected by this Cm-input or Cm-output have their normally defined effect on the function of the element. If a Cm-input or Cm-output stands at its internal 0-state, the inputs affected by this Cm-input or Cm-output have no effect on the function of the element. The notes with Table I and symbols 12-14-01 and 12-14-02 apply.

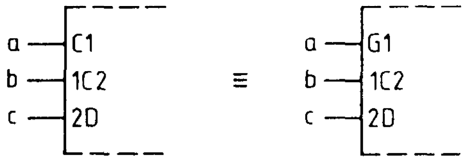
Illustrations







Use has been made of Clause 9.1



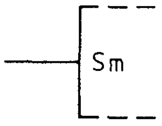
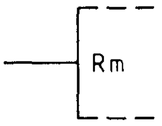
This illustration has been included for explanatory purposes, but the use of a Cm-input to affect a second Cm-input is not recommended.

For comparison of C-, EN- and M-effects on inputs, see Section 22.

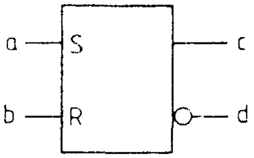
SECTION 19 – SET AND RESET DEPENDENCY (S- AND R-DEPENDENCY)

19.1 SET and RESET dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. These dependencies should not be used if such specification is not necessary.

Affecting S- and R-inputs can affect outputs only.

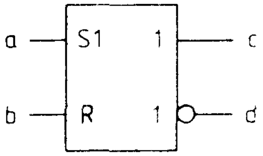
No.	Symbol	Description
12-19-01		Sm-input If an Sm-input stands at its internal 1-state, the outputs affected by this Sm-input will take on the internal logic state they normally would take on for the combination S=1, R=0, regardless of the state of any R-input. If an Sm-input stands at its internal 0-state, it has no effect. The notes with Table I and symbols 12-14-01 and 12-14-02 apply.
12-19-02		Rm-input If an Rm-input stands at its internal 1-state, the outputs affected by this Rm-input will take on the internal logic state they normally would take on for the combination S=0, R=1, regardless of the state of any S-input. If an Rm-input stands at its internal 0-state, it has no effect. The notes with Table I and symbols 12-14-01 and 12-14-02 apply.

Illustrations



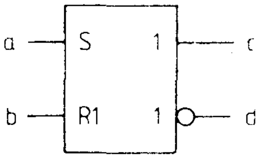
External logic states

a	b	c	d
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	unspecified	



External logic states

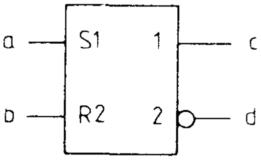
a	b	c	d
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	1	0



External logic state

a	b	c	d
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	0	1

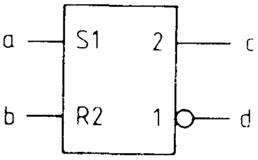
External logic states



a	b	c	d
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	1	1

Note. – The non-complementary output pattern in the last line of the truth table is only pseudo-stable. The simultaneous return of a and b to 0 produces an unforeseeable stable and complementary output pattern.

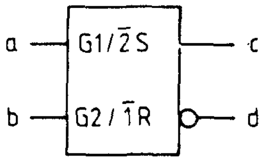
External logic states



a	b	c	d
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	0	0

The note with the preceding illustration applies.

The use of the solidus is explained in Section 25



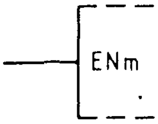
External logic states

a	b	c	d
0	0	unchanged	
0	1	0	1
1	0	1	0
1	1	unchanged	

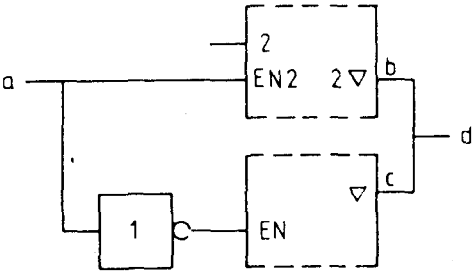
Note. – This example does not use the S- and R-dependencies, but completes the set of alternatives to the unspecified case and demonstrates the fact that S- and R-dependencies cannot affect inputs.

SECTION 20 - ENABLE DEPENDENCY (EN-DEPENDENCY)

20.1 ENABLE dependency is used to indicate an ENABLE input which does not necessarily affect all outputs of an element. It can also be used if one or more inputs of an element are affected.

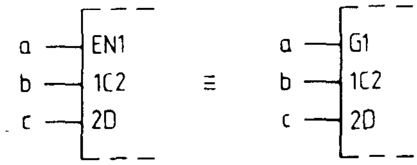
No.	Symbol	Description
12-20-01		ENm-input The effect of this input on its affected outputs is the same as that of a EN-input (see symbol 12-09-11) The effect of this input on its affected inputs is the same as that of an M-input (see symbol 12-21-01). The notes with Table I and symbols 12-14-01 and 12-14-02 apply.

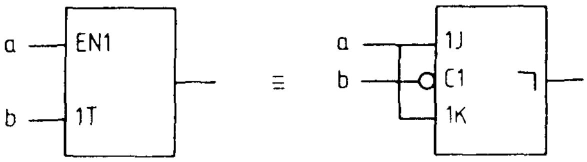
Illustrations



External logic states

a	d
0	c
1	b

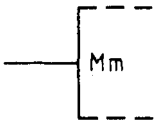
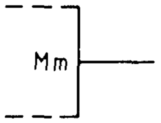




For comparison of C- EN- and M-effects on inputs, see Section 22.

SECTION 21 - MODE DEPENDENCY (M-DEPENDENCY)

21.1 MODE dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

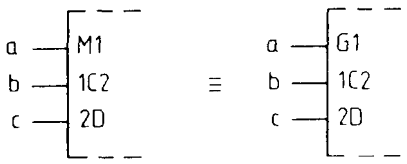
No.	Symbol	Description
12-21-01		Mm-input
12-21-02		Mm-output If an Mm-input or Mm-output stands at its internal 1-state, the inputs affected by this Mm-input or Mm-output have their normally defined effect on the function of the element and the outputs affected by this Mm-input or Mm-output stand at their normally defined internal logic states, i.e. the inputs and outputs are enabled. If an Mm-input or Mm-output stands at its internal 0-state, the inputs affected by this Mm-input or Mm-output have no effect on the function of the element and at each output affected by this Mm-input or Mm-output, any set of labels containing the identifying number of that Mm-input or Mm-output has no effect and is to be ignored. If an affected input has several sets of labels separated by solidi, any set in which the identifying number of the Mm-input or Mm-output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multi-function input. If an output has several sets of labels separated by solidi (see Section 25), only those sets in which the identifying number of this Mm-input or Mm-output appears are to be ignored. This represents disabling or selection of some of the functions of a multi-function output, or the modification of some of the characteristics or dependent relationships of the output. The notes with table 1 and symbol 12-14-01 and 12-14-02 apply.

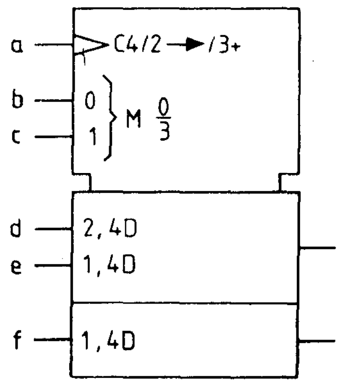
21.2 In complex elements with a large number of different modes, application of the convention for MODE dependency may lead to a very extended labelling. In such cases, the inputs and outputs affected by any affecting M-input are simply labelled with the letter M, but then the diagram containing the symbol must also contain either a table in which the effects of these inputs in the different modes are clearly explained or a statement as to where such a table is to be found. If no confusion can arise, these letters M may be omitted.

Illustrations

The use of the bit-grouping symbol and the solidus is explained in Sections 24 and 25, respectively.

M-dependency affecting inputs:





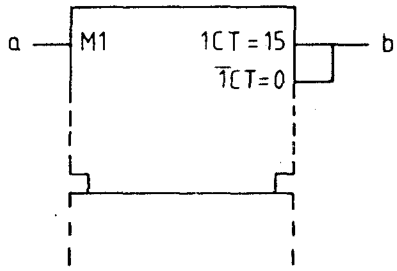
Mode 0 (b = 0, c = 0): the outputs remain at their existing states as none of the inputs has an effect.

Mode I (b = 1, c = 0): parallel loading takes palce through inputs e and f.

Mode 2 (b = 0 , c = 1) : shifting down and serial loading through input d take place.

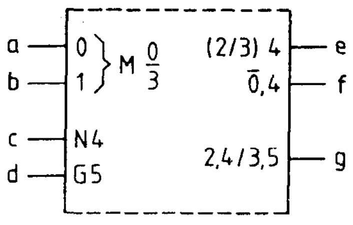
Mode 3 (b = 1, c = 1) : counting up by increment of 1 per clock pulse takes palce (input a).

Determining the function of an output :



If input a stands at its internal 1-state establishing mode 1, output b will stand at its internal 1-state if the content of the register equals 15. If input a stands at its internal 0-state, output b will stand at its internal 1-state if the content of the register equals 0. For explanation, see also Section 25.

Modifying dependent relationships of outputs :



At output e the label set causing negation (if c = 1) is effective in modes 2 and 3 only. In modes 0 and 1, this output stands at its normally defined state as if it had no labels.

At output f the label set has effect if the mode is not 0, so output f is negated (if c = 1) in modes 1, 2 and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example $\overline{0}$, 4 is equivalent to (1/2/3) 4.

At output g there are two label sets. The first set, causing negation (if c = 1), is effective only in mode 2. The second set, subjecting g to AND dependency on d, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so e, f and g will all stand at the same state.

For comparison of C-, EN- and M-effects on inputs, see Section 22.

SECTION 22 - COMPARISON OF C-, EN- AND M-EFFECTS ON INPUTS

With regard to affected input, Cm-, ENm- and Mm-inputs all have the same effect. However, their intended applications are different:

- Cm should be used to identify an input that produces action;
- ENm should be used to identify an input that produces a single preparatory effect;

- Mm should be used to identify one or more inputs that singly or together produce alternative preparatory effects.

SECTION 23 – ADDRESS DEPENDENCY (A-DEPENDENCY)

23.1 ADDRESS dependency provides a clear representation of those elements, particularly memories which use address control inputs to select specified sections of a multidimensional array. ADDRESS dependency allows a symbolic representation of only a single general case of the sections of the array, rather than requiring a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of the selected sections. If any other function than OR is performed, this should be indicated by adding the appropriate qualifying symbol below the general qualifying symbol, e.g. $\begin{matrix}\text{RAM}\\ \& \ \Diamond\end{matrix}$

If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a 3-state output, then this indication refers to the output of the array and not to those of the sections of the array.

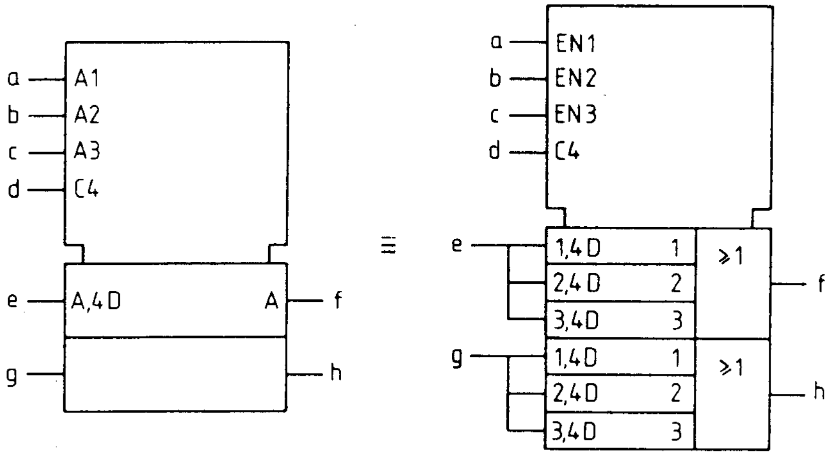
Inputs which are not affected by any affecting ADDRESS input have their normally defined effect on all sections of the array whereas inputs affected by an ADDRESS input have their normally defined effect only on the section selected by the ADDRESS input.

An affecting ADDRESS input is labelled with the letter A followed by an identifying number which corresponds with the address of the particular section of the array selected by this input.

Within the general section presented by the symbol, inputs and outputs affected by an Am-input are labelled with the letter A, which stands for the identifying numbers, i.e. the addresses of the particular sections. This letter A is subject to the rules of dependency notation concerning identifying numbers associated with affected inputs and outputs.

If an output affected by an Am-input also has other labels, then the labels preceding the letter A affect the output of the section selected by this Am-input and the labels placed behind the letter A affect the output of the array i.e. after the application of the OR function (or the indicated function) to the corresponding outputs of the selected sections of the array.

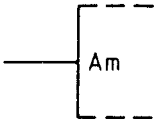
Illustration



23.2 The identifying numbers of affecting ADDRESS inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g. G, V, N, ...) because in the general section presented by the symbol they are replaced by the letter A.

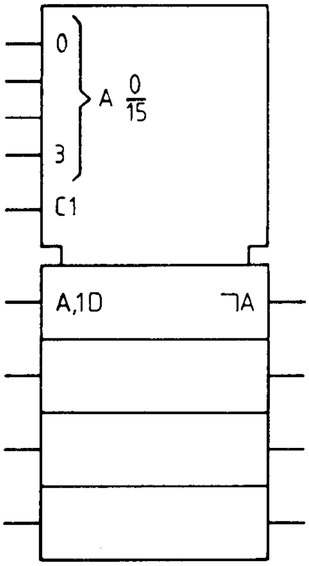
If there are several sets of affecting Am-inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Because they have access to the same sections of the array, these sets of Am-inputs may have the same identifying numbers.

Two affecting ADDRESS inputs having the same identifying number stand in no relation to each other nor to any affecting dependency-input (e.g. Gm, Vm, Nm, ...) having the same identifying number.

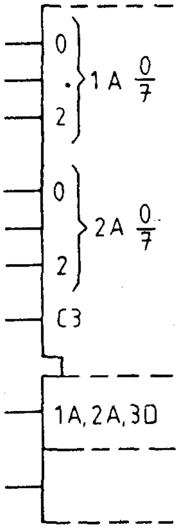
No.	Symbol	Description
12-23-01		Am-input If this input stands at its internal 1-state, the inputs affected by this input (i.e. the inputs of the section of the array selected by this input) have their normally defined effect on the elements of the selected section and the internal logic states of the outputs affected by this input (i.e. the outputs of the selected section) have their normal effect on the OR functions (or the indicated functions determining the internal logic states of the outputs of the array. If the input stands at its internal 0-state, the inputs affected by this input (i.e. the inputs of the section selected by this input) have an effect on the elements of this section and the outputs affected by this input (i.e. the outputs of the section selected by this input) have no effect on the outputs of the array. The notes with Table 1 and symbols 12-14-01 and 12-14-02 apply.

Illustrations

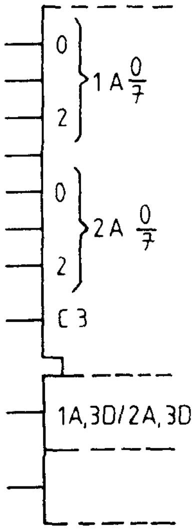
The use of the bit-grouping symbol is explained in Section 24.



Array of 16 sections, each of 4 pulse-triggered D-bistables (see Section 41).

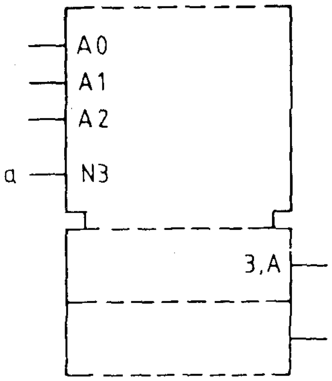


A particular section (among 8) is selected if it is selected by both sets of Am-inputs.



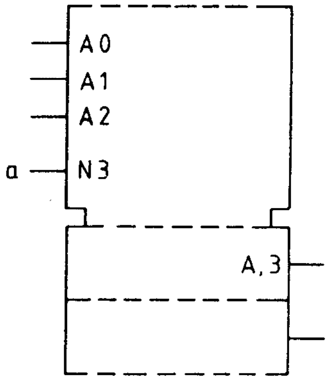
A particular section (among 8) is selected if it is selected either by one or by both sets of Am-inputs.

Suppose a = 1



The internal logic states of the outputs of the array are the results of the OR functions of the complements of the logic states of the outputs of the selected sections.

Suppose a = 1



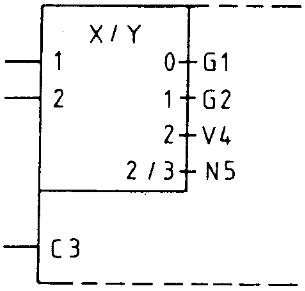
The internal logic states of the outputs of the array are the complements of the results of the OR functions of the logic states of the outputs of the selected sections.

SECTION 24 – SPECIAL TECHNIQUES USED IN DEPENDENCY NOTATION

24.1 Use of a coder to produce affecting inputs

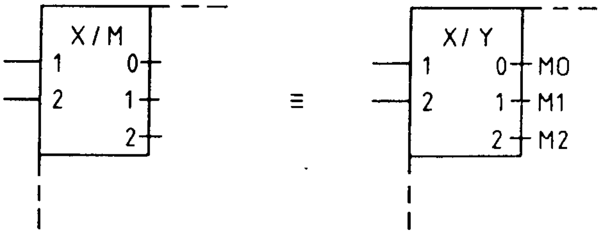
24.1.1 If the effect of a set of affecting inputs is produced by decoding the signals on these inputs, the symbol for a coder (12-32-01) may be used as an embedded symbol.

Illustration



24.1.2 If all affecting inputs produced by a coder are of the same type and if their identifying numbers correspond with the numbers shown at the outputs of the coder, the Y in the qualifying symbol X/Y may be replaced by the letter denoting the type of dependency and the indications of the affecting inputs should then be omitted.

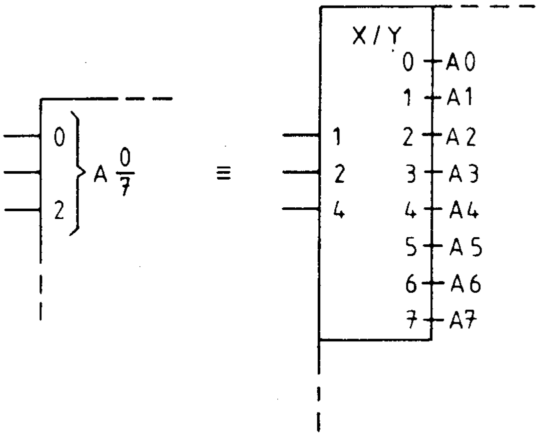
Illustration

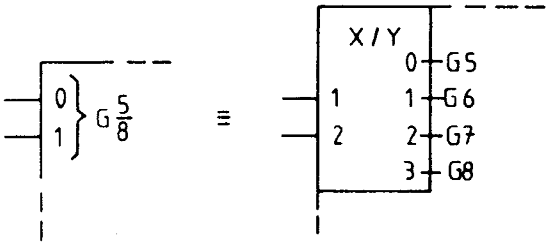


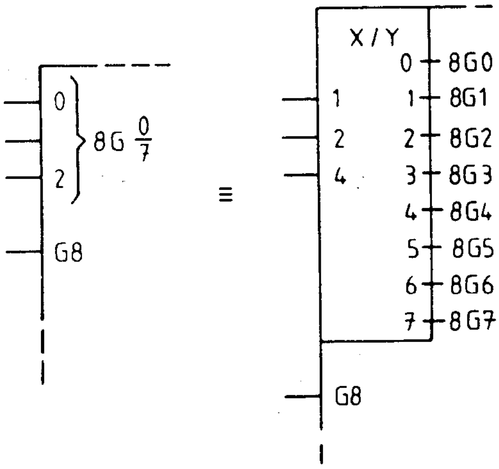
24.2 Use of bit grouping to produce affecting inputs

24.2.1 If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers (not necessarily corresponding with the numbers that would have been shown at the outputs of the coder), the bit grouping symbol (symbol 12-09-24) can be used. In this case, the asterisk shall be replaced by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 shall be replaced by the smallest identifying number and the m2 shall be replaced by the largest. The range of the identifying numbers (m2 – m1 +1) must equal the number of outputs of the coder.

Illustrations







24.3 Designation of labelled inputs having inherent storage

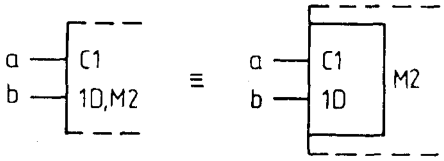
24.3.1 It often occurs that a labelled input other than a D-input has inherent storage. Such an input may be labelled as:

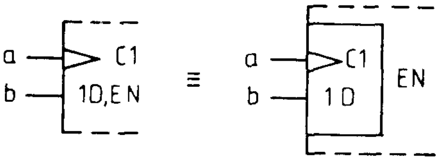
mD,*

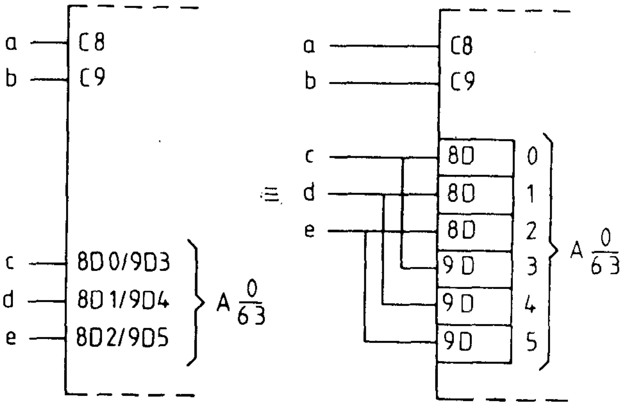
in which

- m shall be replaced by the identifying numbers of the inputs that affect the storage operation;
- the asterisk shall be replaced by the symbol denoting the function of the stored input. If that symbol is a number, the comma following the D may be omitted.

Illustrations







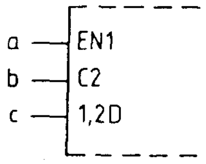
See also Section 25.

SECTION 25 – THE ORDERING OF LABELS ASSOCIATED WITH INPUTS AND WITH OUTPUTS

25.1 Order of input labels

25.1.1 If an input exerting a single function is affected, by other inputs the qualifying symbol for that function shall be preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels shall be the order in which the effects or modifications must be applied. The affected input exerts no function if the logic state of any one of the affecting inputs or outputs, considered separately , would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

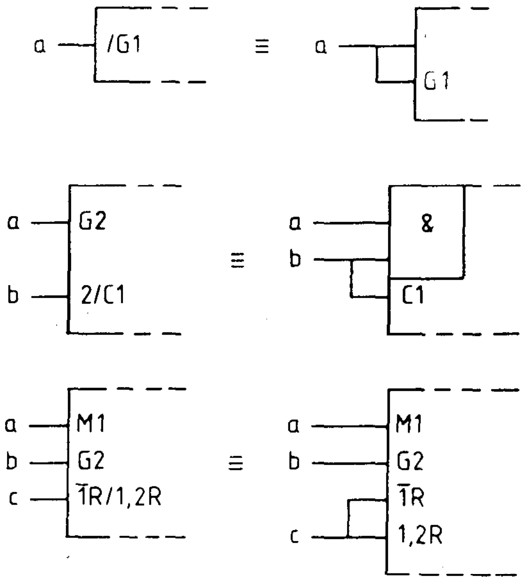
Illustration



If either a = 0 or b = 0, then c has no effect.

25.1.2 If an input exerts more than one function or has more than one set of labels of affecting inputs, the indications of these functions or these sets may be shown on different input lines, which must be connected together outside the outline (see examples 12-33-07, 12-49-11, 12-49-15). However, there are cases in which this method of presentation is not advantageous. In those cases, the input may be shown once with the different sets of labels separated by solidi. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus shall precede the first set of labels shown (see e.g. symbol 12-49-13).

Illustrations

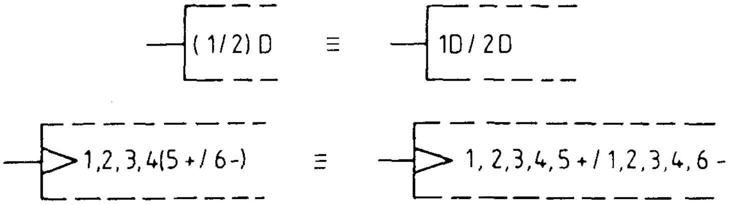


25.1.3 If all inputs of a combinative element are disabled (caused to have no effect on the function on the element), the internal logic states of the outputs of the element are not specified by the symbol.

If all inputs of a sequential element are disabled (caused to have no effect on the function of the element), the content of this element is not changed and the outputs remain at their existing internal logic states.

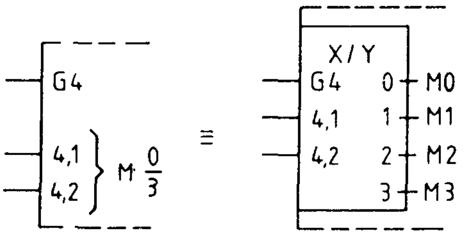
25.1.4 Labels may be factored using algebraic techniques.

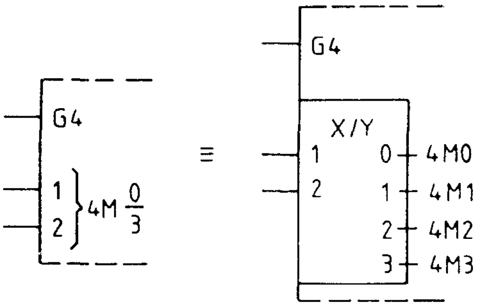
Illustrations



25.1.5 If, at inputs without inherent storage, algebraic factoring techniques are combined with the use of the bit grouping symbol, labels common to all inputs may be shown behind the bit grouping symbol provided the proper order of all labels is maintained.

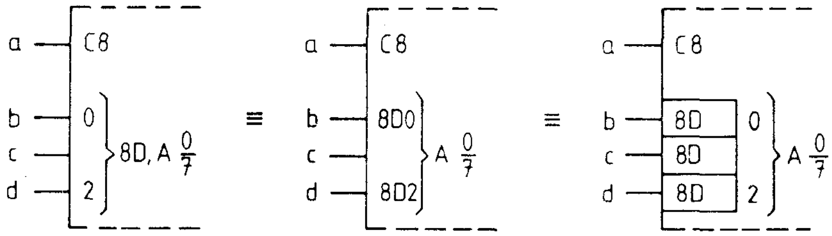
Illustrations





25.1.6 If, at inputs having inherent storage, algebraic factoring techniques are combined with the use of the bit grouping symbol, the indication "mD,", as defined in Clause 24.3, may also be placed behind the bit grouping symbol provided the proper order of all other labels is maintained.

Illustration



25.2 Order of output labels

25.2.1 If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels shall be shown in the following order:

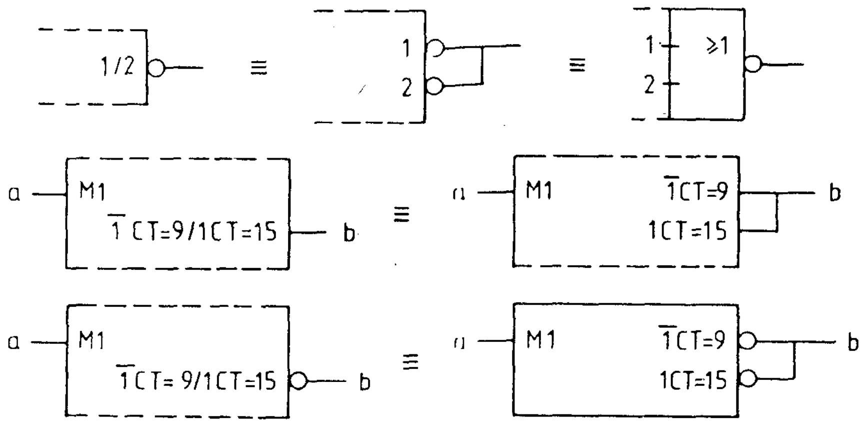
- if the postponed output symbol (12-09-01) has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;
- followed by the qualifying symbols determining or modifying the internal logic state of the output, such that the left-to-right order of these labels correspond with the order in which their effects must be applied for application, see symbol 12-49-15;
- followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit, passive-pull-down, passive-pull-up, or 3-state outputs shall be drawn adjacent to the output line, except when using the bit grouping symbol as described in Sub-clause 25.2.3.

If an output needs several different sets of labels which can be considered to stand in an internal OR relationship (e.g. depending on the mode of action), these sets may be shown on different output lines which must be connected together outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi.

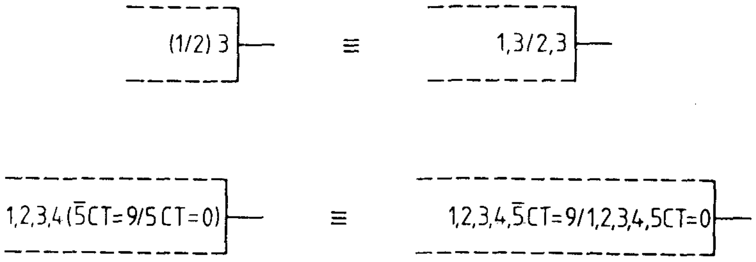
Two adjacent identifying numbers of affecting inputs in a set of labels not already separated by a non-numeric character should be separated by comma (see Section 12).

Illustrations



25.2.2 Labels may also be factored using algebraic techniques.

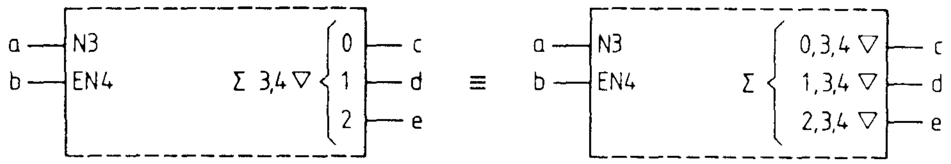
Illustrations


(1/2) 3
≡
1,3/2,3
1,2,3,4($\overline{5}$CT=9/5CT=0)
≡
1,2,3,4,$\overline{5}$CT=9/1,2,3,4,5CT=0

25.2.3 If the bit grouping symbol for outputs (symbol 12-09-25) is used and the sets of labels of all outputs grouped together differ only in the indications of the weights, the sets of labels, including the symbols for open-circuit, passive-pull-down, passive-pull-up or 3-state outputs (symbols 12-09-03 through 12-09-08) but excluding the indications of the weights, may be shown only once between the symbol replacing the asterisk and the grouping symbol, provided that, except for the grouping symbol and the weights, the proper order of the labels is maintained.

Illustration

For the meaning of Σ, see symbol 12-38-01.



CHAPTER V : COMBINATIVE AND SEQUENTIAL ELEMENTS

SECTION 26 – GENERAL NOTES

26.1 All qualifying symbols inside the outline are defined in terms of the internal logic states of the relevant inputs and outputs (see Sections 1, 2 and 3),

26.2 Many of the following examples are based on commercially available devices. Where the polarity indicator has not been used, the positive logic convention is assumed.

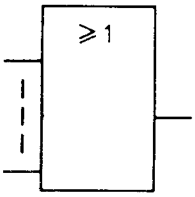
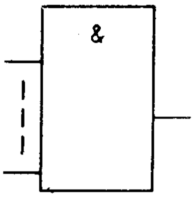
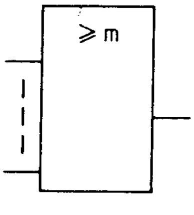
26.3 For the assistance of the reader pin numbers and type numbers have been shown. Where the type number implies the product of a specific manufacturer, this is done to avoid uncertainties caused by functional variations that sometimes occur between devices with the same type number made by different manufacturers.

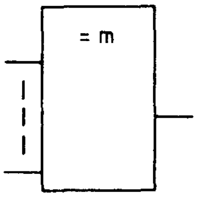
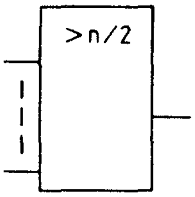
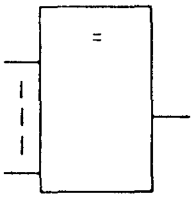
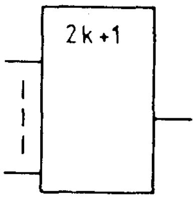
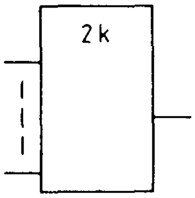
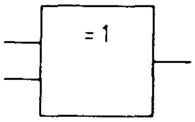
26.4 A given element may be symbolized in more than one way depending on the purpose it serves in the system (e.g. symbols 12-28-10 and 12-28-11). Also, use is often made of the complementary representation especially of combinative elements to enhance the understanding of the diagram, for example an OR element is shown by the symbol for an AND but with negated inputs and outputs. In any case, the choice of the symbol should be governed by the relevant application of the element being shown on the diagram (see IEC publication 113-7 for detailed information).

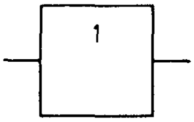
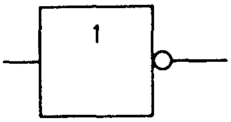
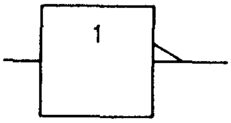
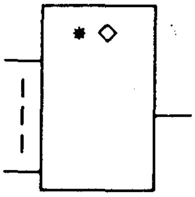
SECTION 27 – COMBINATIVE ELEMENTS

27.1 Convention

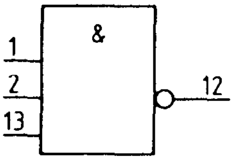
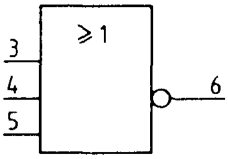
The qualifying symbol for the function of the element indicates the number of inputs which must take on the internal 1-state to cause the outputs to take on their internal 1-states. Subject to this rule, other qualifying symbols than those shown in this section may be developed.

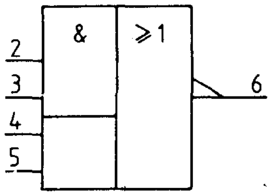
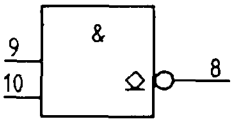
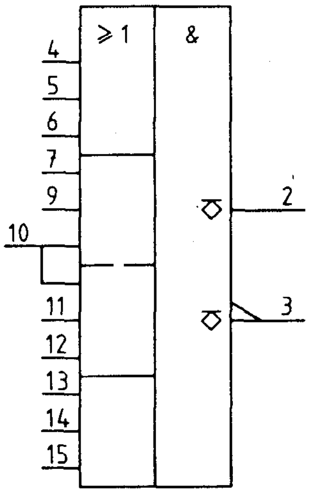
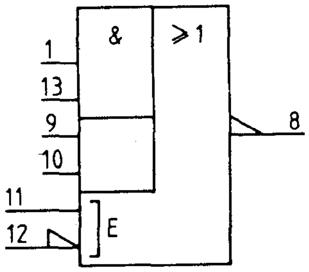
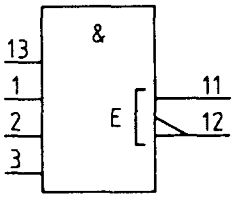
No.	Symbol	Description
12-27-01		OR element, general symbol The output stands at its 1-state if and only if one or more of the input stand at their 1-states. *Note.* – "≥ 1" maay be replaced by "1" if no ambiguity arises.
12-27-02		AND element, general symbol The output stands at its 1-state if and only if all inputs stand at their 1-states.
12-27-03		Logic threshold element, general symbol The output stands at its 1-state if and only if the number of inputs which stand at their 1-states is equal to or greater than the number in the qualifying symbol, represented here by m. *Notes 1.* – m shall always be smaller than the number of inputs. *2.* – An element with m=1 is generally known as OR element (see symbol 12-27-01).

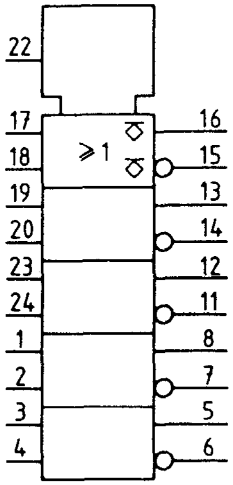
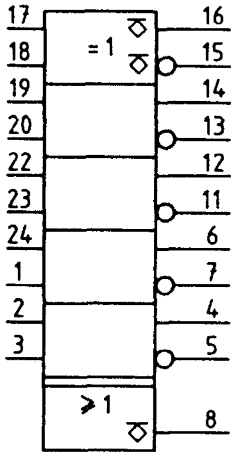
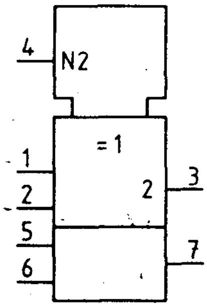
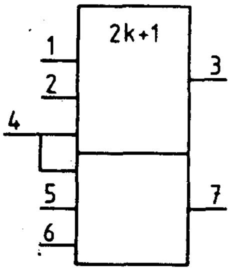
No.	Symbol	Description
12-27-04		m and only m element, general symbol The output stands at its 1-state if and only if the number of inputs which stand at their 1-states is equal to the number in the qualifying symbol, represented here by m. Note 1 with symbol 12-27-03 applies. *Note.* – A 2-input element with m = 1 is generally known as an exclusive-OR element (see symbol 12-27-09).
12-27-05		Majority element, general symbol The output stands at its 1-state if and only if the majority of the inputs stand at their 1-states.
12-27-06		LOGIC IDENTITY element, general symbol The output stands at its 1-state if and only if all inputs stand at the same logic state.
12-27-07		ODD element (ODD-parity element) } Addition modulo 2 element } general symbol The output stands at its 1-state if and only if the number of inputs which stand at their 1-states is odd (1, 3, 5 etc).
12-27-08		EVEN element (EVEN parity element), general symbol The output stands at its 1-state if and only if the number of inputs which stand at their 1-states is even (0, 2, 4, etc).
12-27-09		Exclusive-OR element The output stands at its 1-state if one and only one of the two inputs stands at its 1-state. *Note.* – In the case of more than two inputs, either symbol 12-27-04 with m = 1 or symbol 12-27-07 shall be used depending on the function involved.

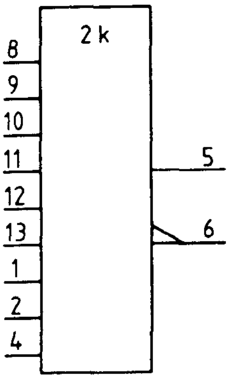
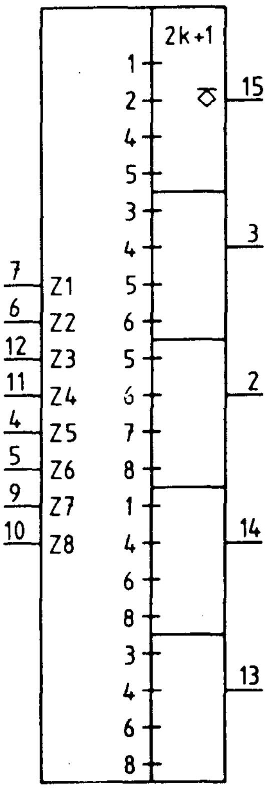
No.	Symbol	Description
12-27-10		Buffer without specially amplified output The output stands at its 1-state if and only if the input stand at its 1-state.
12-27-11		Negator Inverter (in the case of device representation using the logic negation symbol). The output stands at its external 0-state if and only if the input stands at its external 1-state.
12-27-12		Inverter (in the case of device representation using the qualifying symbol for logic polarity). The output stands at its L-level if and only if the input stands at its H-level.
12-27-13		Distributed connection } Dot function } general symbol Wired function } A distributed connection is a connection of specific outputs of a number of elements which are joined together to achieve either the AND- of the OR- function. *Note.* – The asterisk shall be replaced by the qualifying symbol for the function, i.e. & or ≥ 1. As an alternative to the use of the general symbol, a distributed connection may be shown by one of the symbols for a junction of conductors (03-02-04 and 03-02-05). At each point where lines are joined together the qualifying symbol for the function, i.e. & or ≥ 1, shall be shown unless no confusion can arise from its omission.

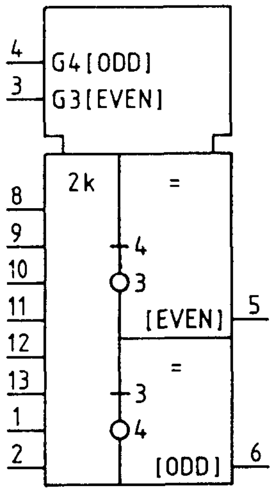
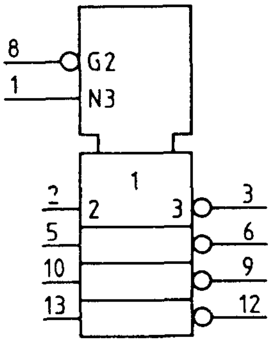
SECTION 28 – EXAMPLES OF COMBINATIVE ELEMENTS

No.	Symbol	Description
12-28-01		AND with negated output (NAND) (e.g. part of SN 7410)
12-28-02		OR with negated output (NOR) (e.g. part of SN 7427)

No.	Symbol	Description
12-28-03		AND-OR-Invert (e.g. part of SN 74L51)
12-28-04		NAND with open-circuit output of the L-type (e.g. part of SN 7403)
12-28-05	 ⩾1 & 4 5 6 7 9 10 11 12 13 14 15 2 3	OR-AND with complementary open-circuit outputs of the H-type (e.g. MC 10121)
12-28-06		AND-OR-Invert, expandable (e.g. part of SN 7450) *Note.* – The line grouping symbol (12-09-47) indicates that two wires are needed to implement the single extension connection.
12-28-07		Expander (e.g. part of SN 7460)

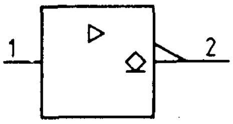
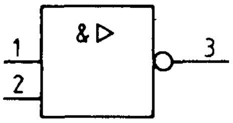
No.	Symbol	Description
12-28-08	 22 17 18 19 20 23 24 1 2 3 4 ≥1 16 15 13 14 12 11 8 7 5 6	OR, with one common input and with complementary outputs, quint (e.g. F 100102)
12-28-09	 17 18 19 20 22 23 24 1 2 3 =1 ≥1 16 15 14 13 12 11 6 7 4 5 8	Exclusive- OR, with complementary outputs and one common output, quint (e.g. E 100107) *Note.* – One output of each of the five elements is internally connected to an input of the common output element. The internal logic state of this input corresponds with that of the output to which it is connected and does not depend on the choice of that output because both outputs of each element have identical internal logic states (see Section 6).
12-28-10		Exclusive- OR/NOR, dual (e.g. part of SN 74S135) *Note.* – Attention is drawn to the fact that symbol 12-28-11 depicts the same device in another way.
12-28-11		ODD element, with one common input, dual (e.g. part of SN 74S135) *Note.* – Attention is drawn to the fact that symbol 12-28-10 depicts the same device in another way.

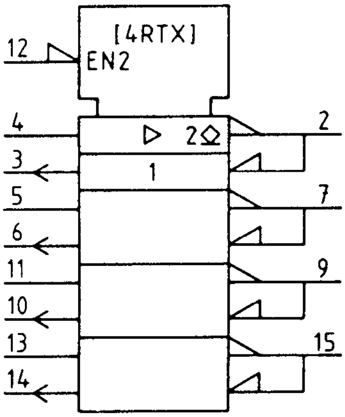
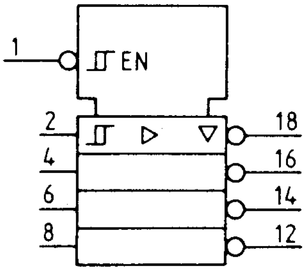
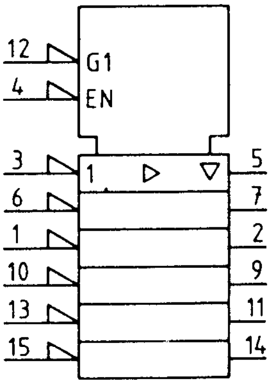
No.	Symbol	Description
12-28-12	 2k 8 9 10 11 12 13 1 2 4 5 6	Parity generator/checker with complementary outputs (e.g. SN 74280)
12-28-13	 2k+1 1 2 4 5 3 4 5 6 5 6 7 8 1 4 6 8 3 4 6 8 15 3 2 14 13 7 6 12 11 4 5 9 10 Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8	Error detection/correction element (e.g. MC 10163)

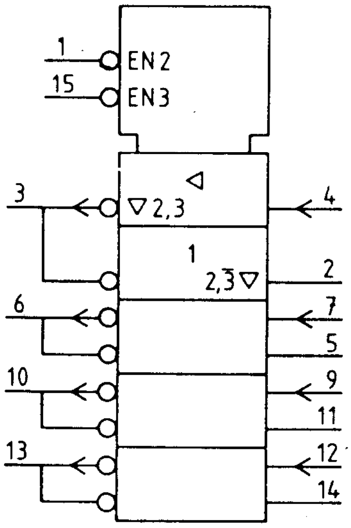
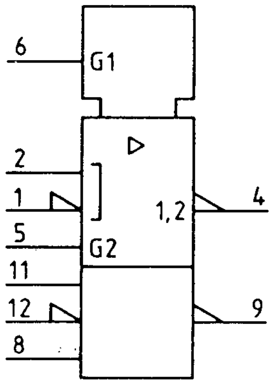
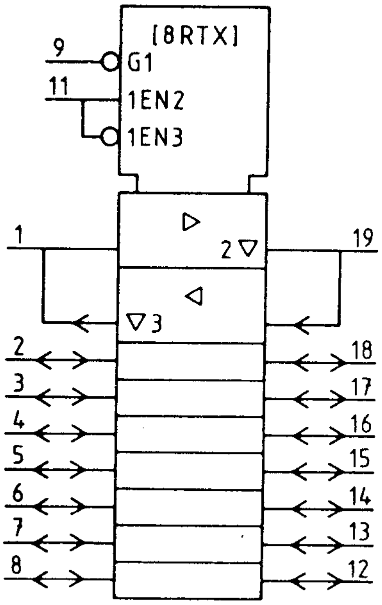
No.	Symbol	Description
12-28-14	 4 3 G4[ODD] G3[EVEN] 2k = 8 9 10 11 12 13 1 2 4 3 [EVEN] 5 = 3 4 [ODD] 6	Parity generator/checker, odd/even (e.g. SN 74180)
12-28-15	 8 1 G2 N3 1 2 2 3 3 5 6 10 9 13 12	True/complement, zero/one element, quad (e.g. SN 74H87)

SECTION 29 – EXAMPLES OF BUFFERS, DRIVERS AND RECEIVERS

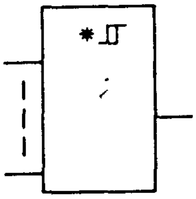
29.1 The symbol for an amplifier (10-15-01) may be combined with other symbols for functions, as shown in this section.

No.	Symbol	Description
12-29-01		Buffer/driver with inverted open-circuit output of the L-type (e.g. part of SN 7406)
12-09-02		NAND buffer (e.g. part of SN 7437)

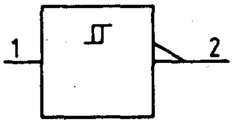
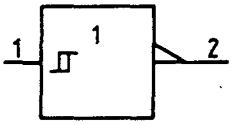
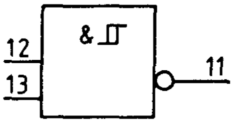
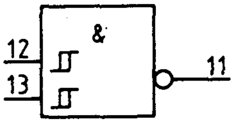
No.	Symbol	Description
12-29-03	 [4RTX] 12 EN2 4 2 3 1 5 7 6 11 9 10 13 15 14	Bus transceiver, quad (e.g. Am 26S10) *Note.* – The general qualifying symbols and those associated with the inputs and outputs of the two outlines forming the first element of the array have been omitted from the remaining elements of the array in accordance with Section 6.
12-29-04		Bus driver with bi-threshold inputs and 3-state outputs, quad (e.g. part of SN 74S240)
12-29-05	 12 G1 4 EN 3 1 5 6 7 1 2 10 9 13 11 15 14	Buffer, inverting, with 3-state outputs, hex (e.g. CD 4502B)

No.	Symbol	Description
12-29-06	 1 15 EN2 EN3 ◁ ▽2,3 3 4 1 2,3▽ 2 6 7 5 10 9 11 13 12 14	Bus driver, bidirectional, quad (e.g. 8226) *Note.* – Pin 1 could be labelled as en EN-input (symbol 12-09-11) without dependency notation, that is, the identifying number 2 may be omitted at three places inside the outline.
12-29-07	 6 G1 ▷ 2 1 5 G2 1,2 4 11 12 8 9	Line receiver, dual (e.g. SN 75107)
12-29-08	 [8RTX] 9 G1 11 1EN2 1EN3 ▷ 2▽ 1 19 ◁ ▽3 2 18 3 17 4 16 5 15 6 14 7 13 8 12	Bus driver, bidirectional, 8-bit parallel (e.g. 8286)

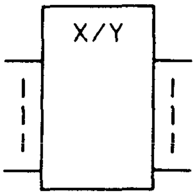
SECTION 30 – ELEMENTS WITH HYSTERESIS

No.	Symbol	Description
12-30-01		Element with hysteresis, general symbol When used within an element as a general qualifying symbol, the hysteresis symbol, ⎎, designates an element whose overall input/output characteristics include hysteresis as described by symbol 12-09-02. The asterisk must be replaced by a general qualifying symbol designating the logic function of the element unless that qualifying symbol is the numeral 1 (of symbol 12-27-10) in which case it shall be omitted.

SECTION 31 – EXAMPLES OF ELEMENTS WITH HYSTERESIS

No.	Symbol	Description
12-31-01		Bi-threshold detector with inverted output Schmitt-trigger inverter Inverter with hysteresis (e.g. part of SN 74LS14) *Note.* – In accordance with the description of symbol 12-09-02, symbol 12-31-01 is equivalent to: 
12-31-02		NAND Schmitt-trigger NAND with hysteresis (e.g. part of SN 74132) The output takes on its internal 1-state only when the external level applied to each input reaches its V1 threshold (see description of symbol 12-09-02). The output will maintain the internal 1-state until the external level applied to one of its inputs reaches its V2 threshold. *Note.* – This symbol is not equivalent to: 

SECTION 32 - CODERS, CODE CONVERTERS

No.	Symbol	Description
12-32-01		Coder, general symbol Code converter, general symbol *Note.* – X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs respectively.

32.1 Relation between inputs and outputs of coders

32.1.1 Indication of code conversion is based on the following rule:

- Depending on the input code the internal logic states of the inputs determine an internal number. This internal number is reproduced by the internal logic states of the outputs, depending on the output code.

  The relationship between the internal logic states of the inputs and the internal number is indicated either by:

- labelling the inputs with numbers, in which case the internal number equals the sum of the numbers associated with those inputs which stand at their internal 1-states;

or by:

- replacing X by a appropriate designation of the input code and labelling the inputs with characters which refer to this code.

  The relationships between the internal number and the internal logic states of the outputs are indicated either by:

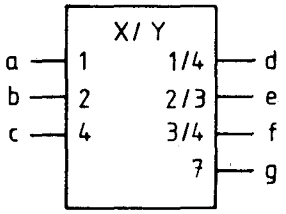
- labelling each output with a list of those internal numbers which lead to the internal 1-state of that output. These internal numbers shall be separated by solidi. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see also Section 24). If a continuous range of internal numbers produces the internal 1-state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, for example:

  4 ... 9 = 4/5/6/7/8/9

or by:

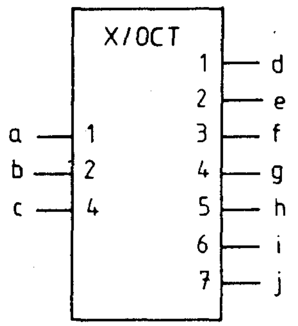
- replacing Y by an appropriate indication of the output code and labelling the outputs with characters which refer to this code.

Illustrations



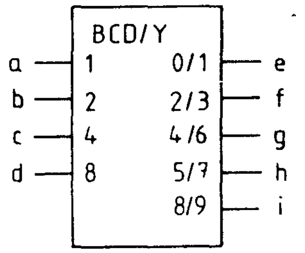
Output d stands at its internal 1-state for the following combinations of internal logic states at inputs a, b and c:

a = 1 b = 0 c = 0
a = 0 b = 0 c = 1



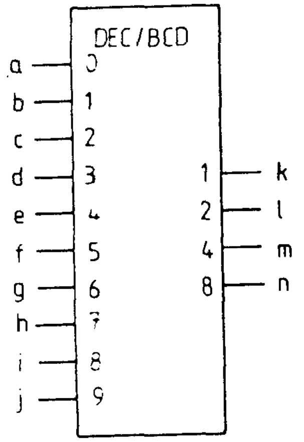
Output h stands at its internal 1-state for the following combination of internal logic states at inputs a, b and c:

a = 1 b = 0 c = 1



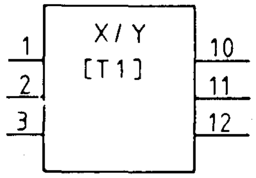
Output i stands at its internal 1-state for the following combinations of internal logic states at inputs a, b, c and d:

a = 0 b = 0 c = 0 d = 1
a = 1 b = 0 c = 0 d = 1



If input j stands at its internal 1-state, outputs k and n stand at their internal 1-states.

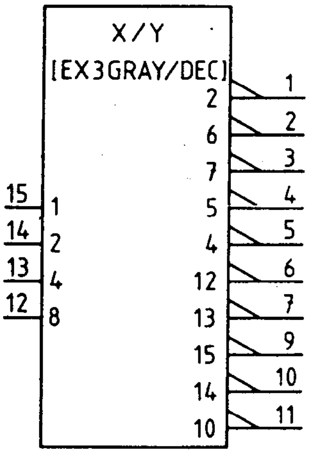
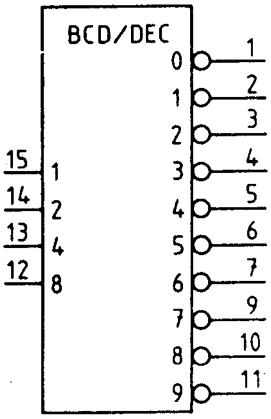
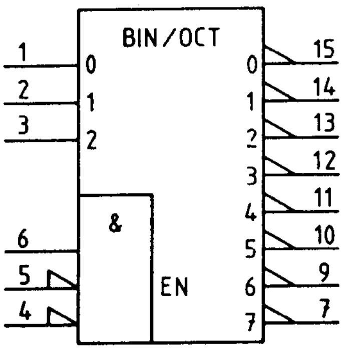
32.1.2 Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. The correspondence between inputs [outputs] and the columns in the table may be given in any convenient way, for example by using pin numbers. In this case any internal labelling which might be confused with that arising in one of the other methods must be avoided.

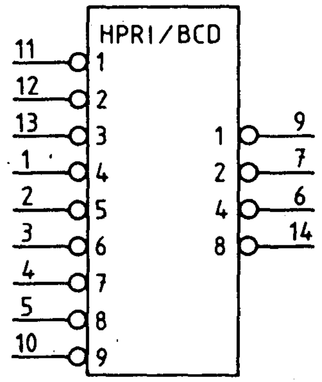
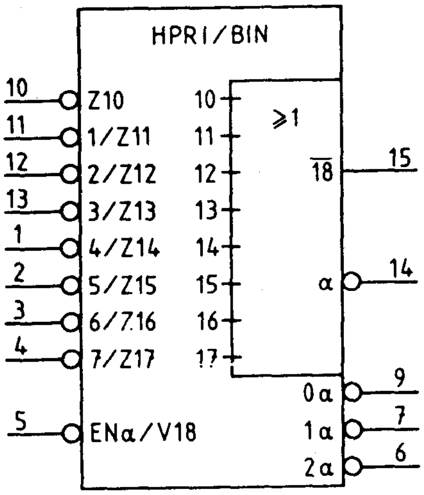
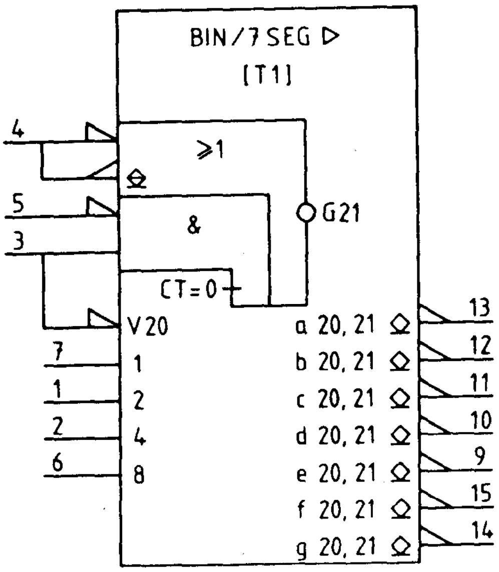
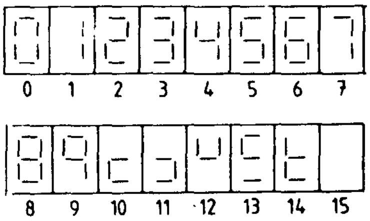
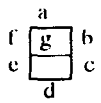


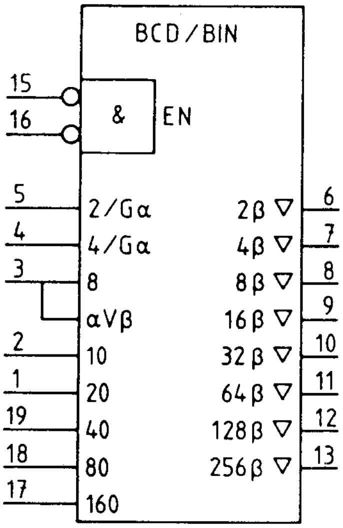
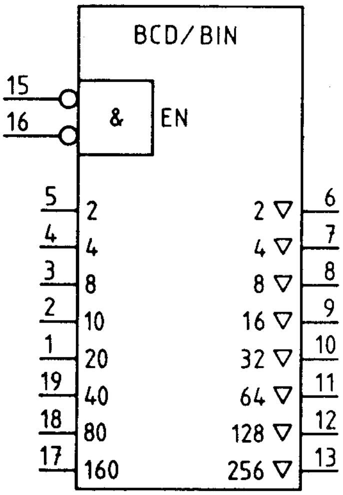
T1

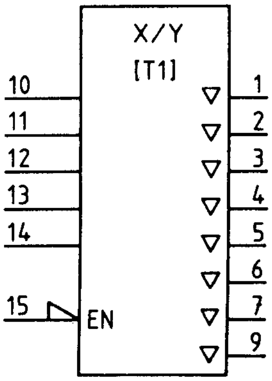
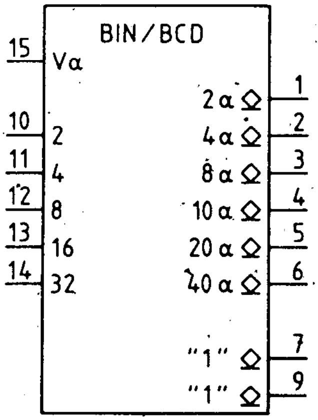
Inputs			Outputs		
1	2	3	10	11	12
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	0	0	0

SECTION 33 – EXAMPLES OF CODE CONVERTERS

No.	Symbol	Description
12-33-01	 X/Y [EX3GRAY/DEC] 15 1 14 2 13 4 12 8 2 1 6 2 7 3 5 4 4 5 12 6 13 7 15 9 14 10 10 11	Code converter, excess-3 Gray-to-decimal (e.g. SN 7444) *Note.* – Because it is not possible to label the inputs with characters referring to the excess-3-Gray code, the general symbol for a coder is shown here in accordance with the first alternative of the second and the third paragraphs of Sub-clause 32.1.1.
12-33-02	 BCD/DEC 15 1 14 2 13 4 12 8 0 1 1 2 2 3 3 4 4 5 5 6 6 7 7 9 8 10 9 11	Code converter, BCD-to-decimal (e.g. SN 7442)
12-33-03	 BIN/OCT 1 0 2 1 3 2 & 6 5 4 EN 0 15 1 14 2 13 3 12 4 11 5 10 6 9 7 7	Code converter, three-to-eight-line (e.g. SN 74LS138) *Note.* – Attention is drawn to the fact that symbol 12-37-04 depicts the same device in another way.

No.	Symbol	Description
12-33-04	 HPRI/BCD 11 12 13 1 2 3 4 5 10 1 2 3 4 5 6 7 8 9 1 2 4 8 9 7 6 14	Highest priority encoder, encoding 9 data lines to 4-line BCD (e.g. SN 74147)
12-33-05	 HPRI/BIN 10 11 12 13 1 2 3 4 5 Z10 1/Z11 2/Z12 3/Z13 4/Z14 5/Z15 6/Z16 7/Z17 ENα/V18 10 11 12 13 14 15 16 17 ≥1 $\overline{18}$ α 0α 1α 2α 15 14 9 7 6	Highest priority encoder, encoding 8 data lines to 3-line binary (octal) (e.g. SN 74148)
12-33-06	 BIN/7SEG ▷ [T1] 4 5 3 ≥1 & CT=0 G21 V20 7 1 2 6 1 2 4 8 a 20, 21 b 20, 21 c 20, 21 d 20, 21 e 20, 21 f 20, 21 g 20, 21 13 12 11 10 9 15 14	Decoder/driver, BCD-to-seven-segment (e.g. SN 74L47) *Note.* – This example shows the use of the polarity indicator at external connections together with the use of the negation indicator at internal connections (see Section 7). Font Table T1:  0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 Numerical designations and resultant displays Segment identification: 

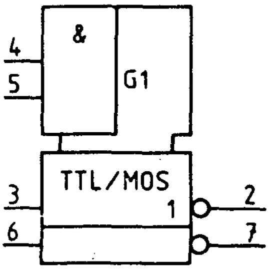
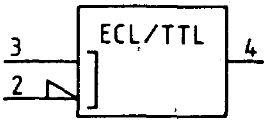
No.	Symbol	Description
12-33-07	 BCD/BIN 15 16 & EN 5 4 3 2 1 19 18 17 2/Gα 4/Gα 8 αVβ 10 20 40 80 160 2β 4β 8β 16β 32β 64β 128β 256β 6 7 8 9 10 11 12 13	Code converter, BCD-to-binary (e.g. SN 74S484)
12-33-08	Simplified form  BCD/BIN 15 16 & EN 5 4 3 2 1 19 18 17 2 4 8 10 20 40 80 160 2 4 8 16 32 64 128 256 6 7 8 9 10 11 12 13	

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>12-33-09</td><td> </td><td>Coder for arbitrary code
(e.g. TBP 18S030, formerly SN 74S288
The combinative relationships between inputs and outputs are implemented in a PROM (or a ROM).
"T1" refers to a table (or to Boolean equations) showing the logic function of the device, for example:
T1
<table>
<tr><th colspan="5">Inputs</th><th colspan="8">Outputs
(with device enabled)</th></tr>
<tr><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>-</td><td>-</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>-</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>-</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>-</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>-</td><td>-</td><td>L</td><td>L</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>-</td><td>-</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>-</td><td>-</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>-</td><td>-</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
</table>
– = irrelevant (don't care)</td></tr>
<tr><td>12-33-10</td><td> </td><td>Code converter, binary-to-BCD
(e. g. SN 74185)</td></tr>
</table>

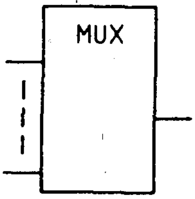
SECTION 34 – SIGNAL-LEVEL CONVERTERS WITH OR WITHOUT GALVANIC SEPARATION

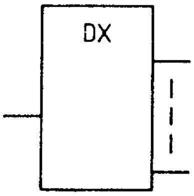
No.	Symbol	Description
12-34-01	Use symbol 12-32-01	Signal-level converter, general symbol The level references may be shown inside the symbol and shall replace X and Y if confusion with the coder can arise. *Note.* – The general qualifying symbol X/Y may be replaced by X//Y if it is necessary to indicate galvanic separation between the inputs and outputs.

SECTION 35 – EXAMPLES OF SIGNAL-LEVEL CONVERTERS

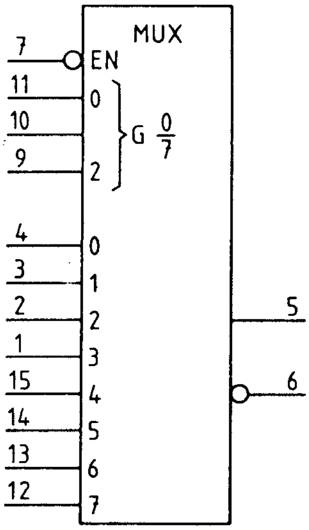
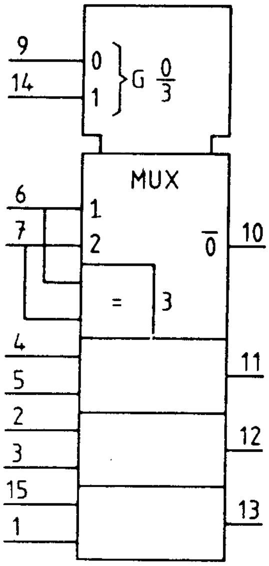
No.	Symbol	Description
12-35-01		Level converter, TTL-to-MOS, dual (e.g. part of SN 75365)
12-35-02		Level converter, ECL-to-TTL (e.g. part of MC 10125)

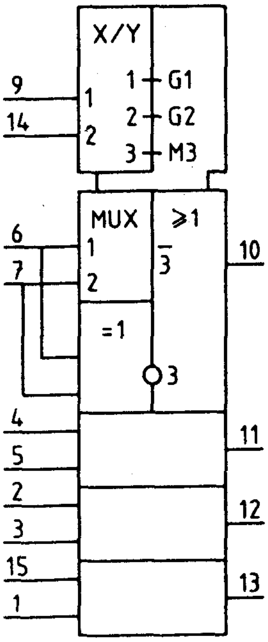
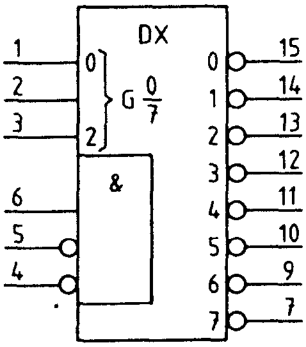
SECTION 36 – MULTIPLEXERS AND DEMULTIPLEXERS

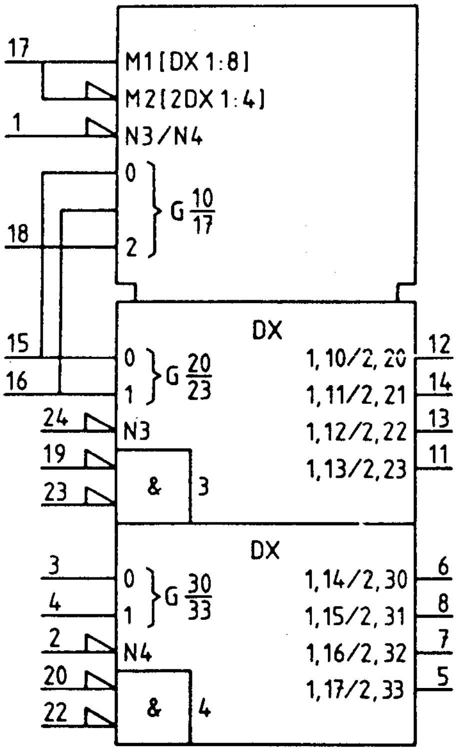
No.	Symbol	Description
12-36-01		Multiplexer, general symbol If one input of a multiplexer is selected, the internal logic state of the output takes on the internal state of the selected input. If no input is selected, the output stands at it internal 0-state: *Note.* – The inputs and logic relationships that control the selecting action must also be shown, for example by showing those inputs and the associated dependency notation either within the element or within a common control block.

No.	Symbol	Description
12-36-02		Demultiplexer, general symbol If an output of a demultiplexer is selected, the internal logic state of that output takes on the internal logic state of the input. Otherwise, the output takes on its internal 0-state. The note with symbol 12-36-01 applies. *Note.* – If confusion can arise, DX may be replaced by DMUX.

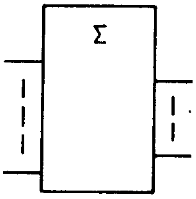
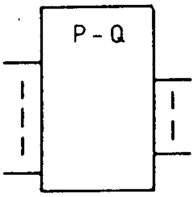
SECTION 37 – EXAMPLES OF MULTIPLEXERS AND DEMULTIPLEXERS

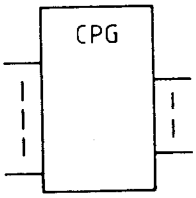
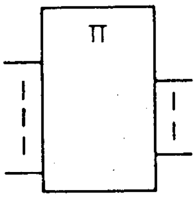
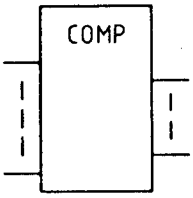
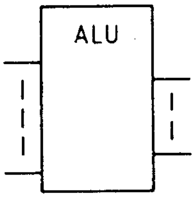
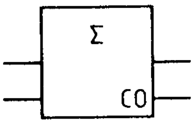
No.	Symbol	Description
12-37-01	 MUX 7 EN 11 10 9 0 2 G 0/7 4 3 2 1 15 14 13 12 0 1 2 3 4 5 6 7 5 6	Multiplexer (one-of-eight) (e.g. SN 74151)
12-37-02	 9 14 0 1 G 0/3 MUX 6 7 1 2 = 3 0̄ 10 4 5 2 3 15 1 11 12 13	Multiplexer, quad (e.g. MC 14519) *Notes. 1.* – 0̄ is optional (see description of symbol 12-36-01). *2.* – Attention is drawn to the fact that symbol 12-37-03 depicts the same device in another way.

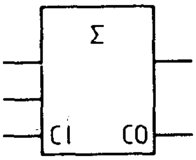
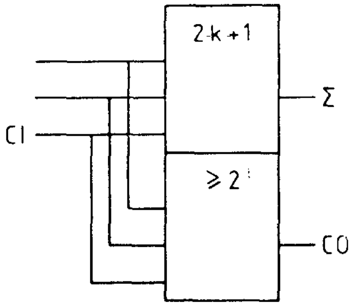
No.	Symbol	Description
12-37-03	 X/Y 9 14 1 2 1 2 3 G1 G2 M3 MUX ≥1 6 7 1 2 $\overline{3}$ 10 =1 3 4 5 11 2 3 12 15 1 13	Exclusive NOR, quad (e.g. MC 14519) *Note.* – Attention is drawn to the fact that symbol 12-37-02 depicts the same device in another way.
12-37-04	 DX 1 2 3 0 2 G $\frac{0}{7}$ & 6 5 4 0 1 2 3 4 5 6 7 15 14 13 12 11 10 9 7	Demultiplexer (one-to-eight) (e.g. SN74LS138) *Note.* – Attention is drawn to the fact that symbol 12-33-03 depicts the same device in another way.

No.	Symbol	Description
12-37-05	 17 M1[DX 1:8] M2[2DX 1:4] 1 N3/N4 0 G 10/17 18 2 DX 15 16 0 1 G 20/23 24 N3 19 23 & 3 1,10/2,20 1,11/2,21 1,12/2,22 1,13/2,23 12 14 13 11 DX 3 4 0 1 G 30/33 2 N4 20 22 & 4 1,14/2,30 1,15/2,31 1,16/2,32 1,17/2,33 6 8 7 5	**Demultiplexer/decoder, universal, dual** (e.g. F 100170) *Notes. 1.* – In order to perform the function DX1:8 correctly, it is necessary to make an external connection between pins 19 and 20, and also between pins 22 and 23. 2. – The symbol for open-circuit output (symbol 12-09-04) is not shown in this example.

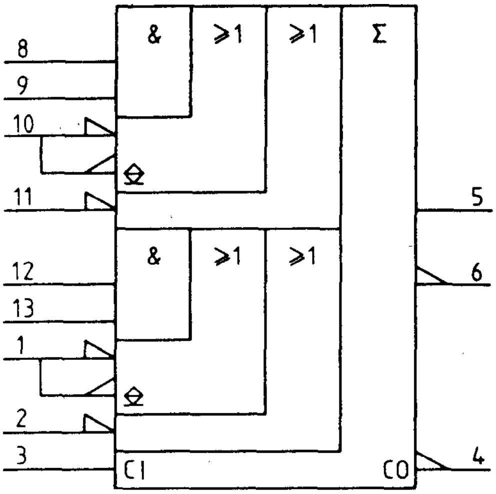
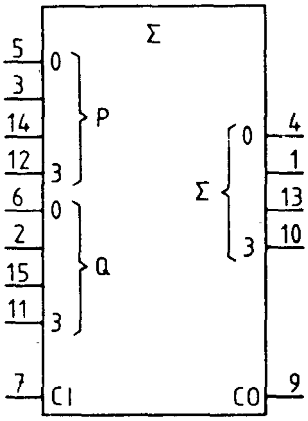
SECTION 38 – ARITHMETIC ELEMENTS

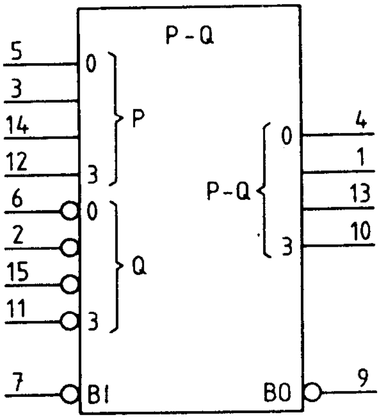
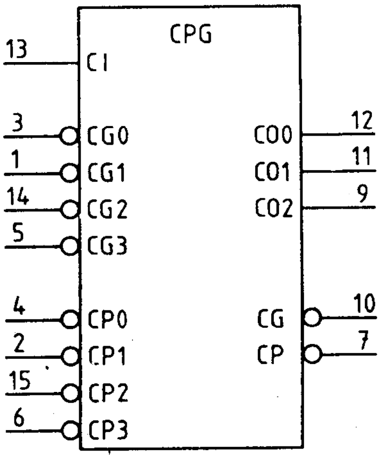
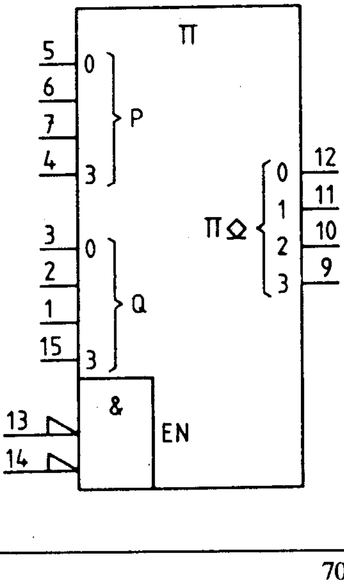
No.	Symbol	Description
12-38-01		Adder, general symbol
12-38-02		Subtractor, general symbol

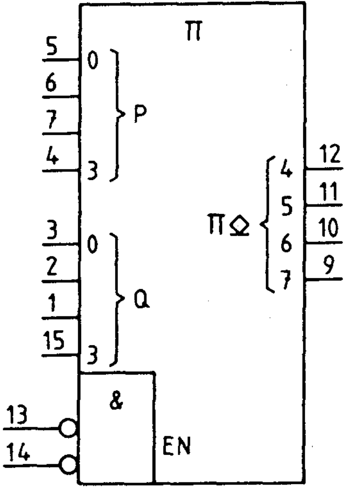
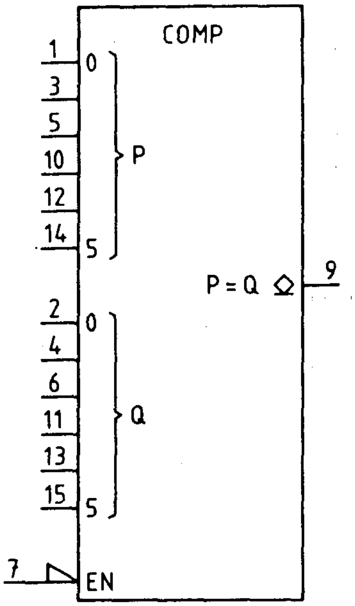
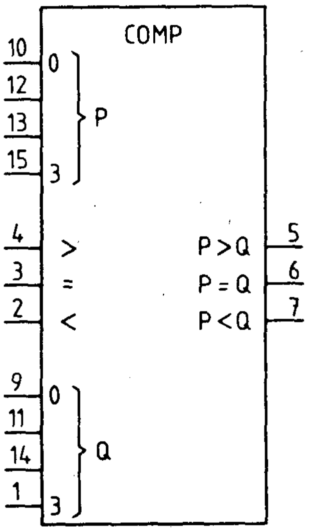
No.	Symbol	Description
12-38-03		Look-ahead carry generator (carry propagate and generate), general symbol
12-38-04		Multiplier, general symbol
12-38-05		Magnitude comparator, general symbol A cascadable comparator is assumed to implement a portion of a comparison that proceeds from lower to higher order, unless otherwise indicated, for example by "[H-L]" placed below the qualifying symbol "COMP".
12-38-06		Arithmetic logic unit, general symbol Supplementary information shall be added to the general qualifying symbol to specify the function of the element (see e.g. symbol 12-39-10)
12-38-07		Half adder

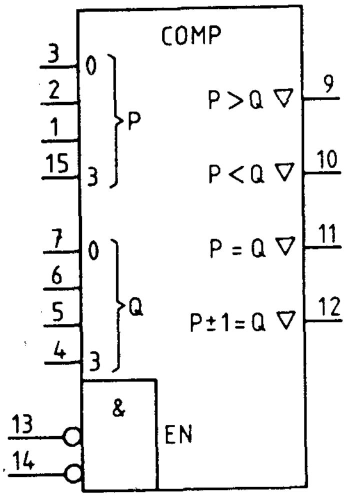
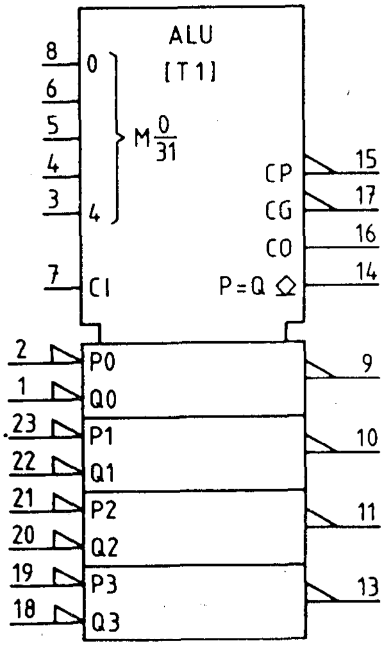
No.	Symbol	Description
12-38-08		Single-bit full adder *Note.* – A simple single-bit full adder may alternatively be depicted by the combination of the symbol for the ODD element (modulo 2 adder) and the logic threshold element as shown below: 

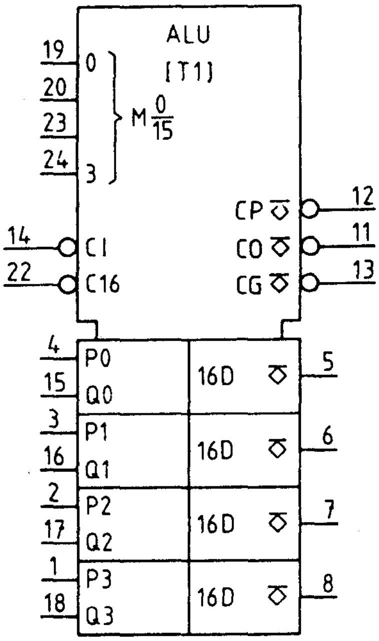
SECTION 39 – EXAMPLES OF ARITHMETIC ELEMENTS

No.	Symbol	Description
12-39-01	 & ≥1 ≥1 Σ 8 9 10 11 5 & ≥1 ≥1 12 13 6 1 2 3 CI CO 4	Single-bit full adder with complementary sum outputs and inverted carry output (e.g. SN 7480)
12-39-02	 Σ 5 3 14 12 0 P 3 6 2 15 11 0 Q 3 Σ 0 3 4 1 13 10 7 CI CO 9	Full adder, 4-bit (e.g. SN 74283) *Note.* – Attention is drawn to the fact that symbol 12-39-03 depicts the same device in another way.

No.	Symbol	Description
12-39-03	 P-Q 5 3 14 12 0 3 P 6 2 15 11 0 3 Q P-Q 0 3 4 1 13 10 7 BI BO 9	Full subtractor, 4-bit (e.g. SN 74283) *Note.* – Attention is drawn to the fact that symbol 12-39-02 depicts the same device in another way.
12-39-04	 CPG 13 CI 3 CG0 1 CG1 14 CG2 5 CG3 4 CP0 2 CP1 15 CP2 6 CP3 CO0 12 CO1 11 CO2 9 CG 10 CP 7	Look-ahead carry generator, 4-bit (e.g. SN 74182)
12-39-05	 π 5 6 7 4 0 3 P 3 2 1 15 0 3 Q πΩ 0 1 2 3 12 11 10 9 & 13 14 EN	Multiplier, 4-bit parallel, generating the four least significant bits of the product (e. g. SN 74285)

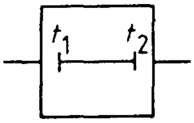
No.	Symbol	Description
12-39-06	 Π 5 6 7 4 0 3 P 3 2 1 15 0 3 Q 13 14 & EN Π◇ 4 5 6 7 12 11 10 9	Multiplier, 4-bit parallel, generating the four most significant bits of the product (e.g. SN 74284)
12-39-07	 COMP 1 3 5 10 12 14 0 5 P P = Q ◇ 9 2 4 6 11 13 15 0 5 Q 7 EN	Magnitude comparator with open-circuit output of the L-type, 6-bit (e.g. DM 7160)
12-39-08	 COMP 10 12 13 15 0 3 P 4 3 2 > = < P>Q P=Q P<Q 5 6 7 9 11 14 1 0 3 Q	Magnitude comparator with cascading inputs, 4-bit (e.g. SN 7485)

No.	Symbol	Description
12-39-09	 COMP 3 2 1 15 0 P 3 7 6 5 4 0 Q 3 P>Q ∇ 9 P<Q ∇ 10 P = Q ∇ 11 P±1=Q ∇ 12 & EN 13 14	Magnitude comparator with 3-state outputs, 4-bit (e.g. DM 76L24)
12-39-10	 ALU [T1] 8 6 5 4 3 0 4 M 0/31 7 CI CP 15 CG 17 CO 16 P=Q 14 2 P0 1 Q0 23 P1 22 Q1 21 P2 20 Q2 19 P3 18 Q3 9 10 11 13	Arithmetic logic unit, 4-bit (e.g. SN 74181) *Notes 1.* - [T1] refers to supplementary documentation detailing the element's function in various modes. *2.* - The M's at the outputs have been omitted in accordance with Clause 21.2.

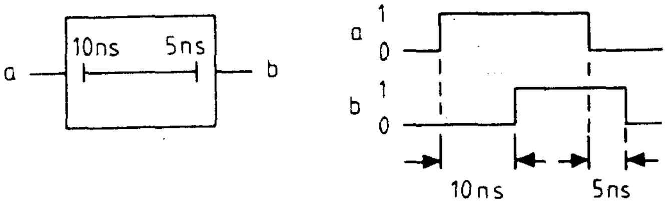
No.	Symbol	Description
12-39-11	 ALU [T1] M $\frac{0}{15}$ 19 20 23 24 0 3 14 22 CI C16 CP CO CG 12 11 13 4 15 3 16 2 17 1 18 P0 Q0 P1 Q1 P2 Q2 P3 Q3 16D 5 6 7 8	Arithmetic logic unit with output latches, 4-bit (e.g. F 100181) The notes with symbol 12-39-10 apply.

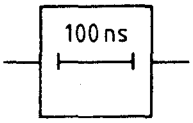
SECTION 40 – BINARY DELAY ELEMENTS

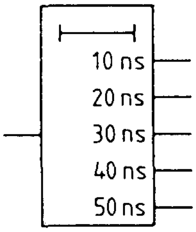
40.1 The qualifying symbol 02-08-05 is also used in the representation of binary delay elements as shown in this section.

No.	Symbol	Description
12-40-01		Delay element with specified delay times A transition from the internal 0-state to the internal 1-state at the output occurs after a delay of t_1 with reference to the same transition at the input. The transition from the internal 1-state to the internal 0-state at the output occurs after a delay of t_2 with reference to the same transition at the input. *Note.* – t_1 and t_2 may be replaced by the actual delays, expressed in seconds, or units or digit units, and may be placed inside word outside the outline. If the two delays are equal, it is sufficient to insert one value only.

Illustration



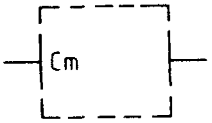
No.	Symbol	Description
12-40-02		Delay element (100 ns)

No.	Symbol	Description
12-40-03		Tapped delay element (in steps of 10 ns)

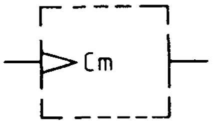
SECTION 41 – BISTABLE ELEMENTS

41.1 The symbol for a bistable element does not contain a general qualifying symbol for the function, the latter being indicated by qualifying symbols associated with the inputs and outputs.

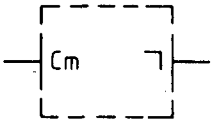
41.2 For bistable elements controlled by Cm-inputs (symbol 12-18-01), it is necessary to distinguish between four types, i.e. latches, edge-triggered bistables, pulse-triggered bistables and data-lock-out bistables. In accordance with the descriptions of the symbols for a dynamic input (12-07-07) and for a postponed output (12-09-01):



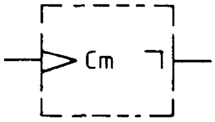
indicates a latch



indicates an edge-triggered bistable



indicates a pulse-triggered bistable

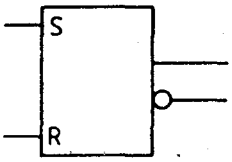
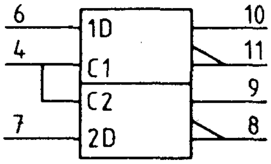
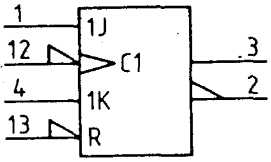
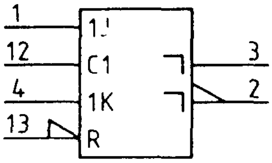
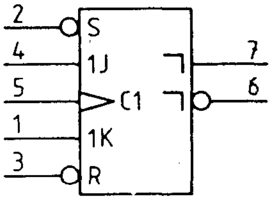
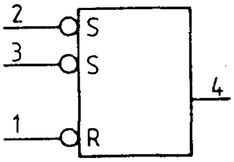


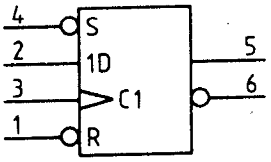
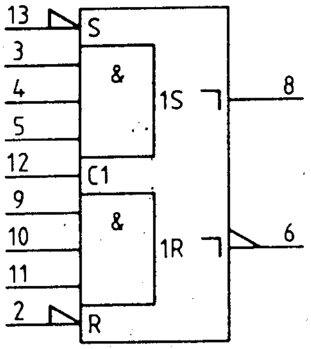
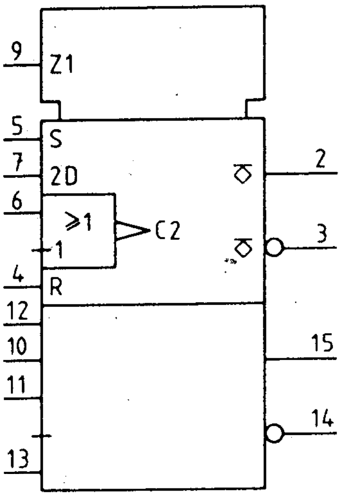
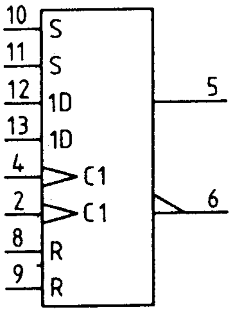
indicates a data-lock-out bistable

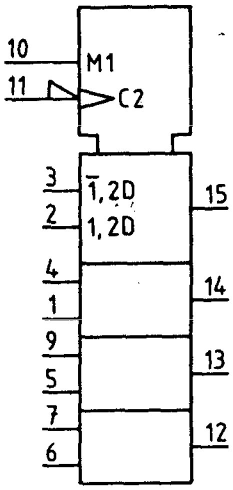
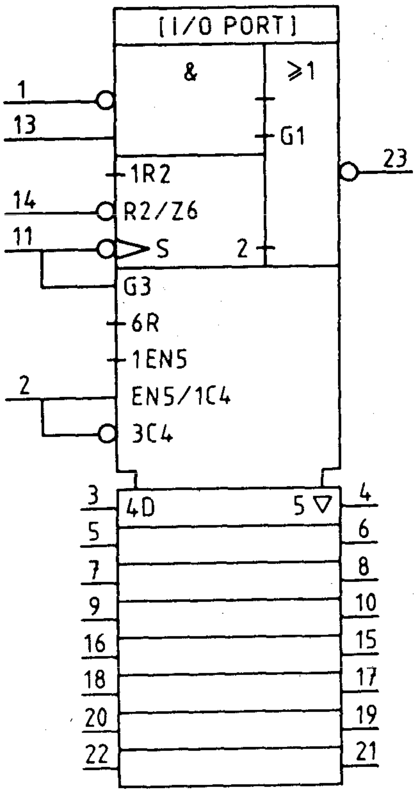
For edge-triggered, pulse-triggered and data-lock-out bistables, the inputs affected by the Cm-input are assumed to be stable during the period that the Cm-input stands at its internal 1- state. If they do change their states during this period, the function of the element is not specified by the symbol.

The same symbology is used for more complex elements such as shift registers and counters to indicate whether they are of the edge-triggered, the pulse-triggered or the data-lock-out type. For elements of the pulse-triggered or the data-lock-out type, if reference is made to the content of the element (e.g. by a CT- output), this content shall be considered as being the content after the application of the postponed output symbol.

SECTION 42 – EXAMPLES OF BISTABLE ELEMENTS

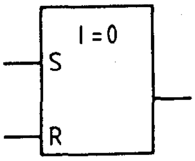
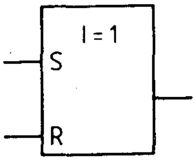
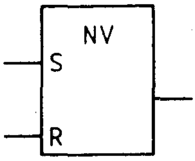
No.	Symbol	Description
12-42-01		RS-bistable RS-latch
12-42-02		D-latch, dual (e.g. part of SN 7475)
12-42-03		Edge-triggered JK-bistable (e.g. part of SN 74LS107)
12-42-04		Pulse-triggered JK-bistable (e.g. part of SN 74107)
12-42-05		Data-lock-out JK-bistable (e.g. part of SN 74111)
12-42-06		RS-latch with negated inputs ($\overline{R}\,\overline{S}$ - latch) (e.g. part of SN 74279)

No.	Symbol	Description
12-42-07		Edge-triggered D-bistable (e.g. part of SN 7474)
12-42-08	 13 S 3 & 4 5 1S 8 12 C1 9 & 10 1R 6 11 2 R	Pulse-triggered RS-bistable (e.g. SN 74L71)
12-42-09	 9 Z1 5 S 7 2D 2 6 ≥1 C2 1 3 4 R 12 10 15 11 14 13	Edge-triggered D-bistable, dual (e.g. MC 10131)
12-42-10	 10 S 11 S 12 1D 5 13 1D 4 C1 2 C1 6 8 R 9 R	Edge-triggered D-bistable (e.g. MC 1222)

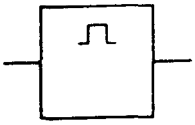
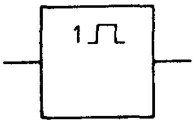
No.	Symbol	Description
12-42-11	 10 M1 11 C2 3 1̄,2D 2 1,2D 15 4 1 14 9 5 13 7 6 12	Multiplexer with storage, quad 2-input (e.g. SN 74298) *Note.* – The "M1" at pin 10 may be replaced by "G1".
12-42-12	 [I/O PORT] & ≥1 1 13 G1 23 1R2 14 R2/Z6 11 S 2 G3 6R 1EN5 2 EN5/1C4 3C4 3 4D 5 ▽ 4 5 6 7 8 9 10 16 15 18 17 20 19 22 21	Input/output port, 8-bit (e.g. 8212)

SECTION 43 – INDICATION OF SPECIAL SWITCHING PROPERTIES OF BISTABLE ELEMENTS

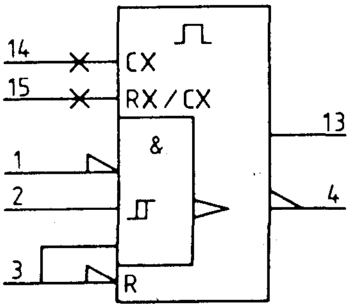
43.1 In some applications (e.g. fail-safe systems) it is necessary to indicate the internal logic state of the outputs of a bistable element at the moment the supply is switched on. The symbols below show how this may be done. The qualifying symbols may be applied to other types of bistable elements.

No.	Symbol	Description
12-43-01		RS-bistable with initial 0-state At the moment the supply is switched on, the output will stand at its internal 0-state.
12-43-02		RS-bistable with initial 1-state At the moment the supply is switched on, the output will stand at its internal 1-state.
12-43-03		RS-bistable, non-volatile At the moment the supply is switched on, the internal logic state of the output will be the same as it was when the supply was switched off.

SECTION 44 – MONOSTABLE ELEMENTS

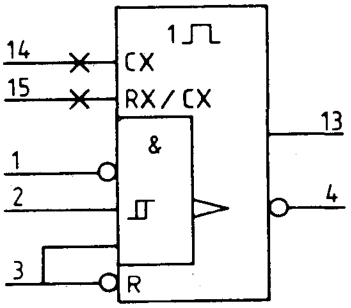
No.	Symbol	Description
12-44-01		Monostable, retriggerable (during the output pulse), general symbol Simple shot, general symbol The output changes to or remains at its 1-state each time the input changes to its 1-state. The output returns to its 0-state after a period of time which is characteristic of the particular device, beginning at the last change of the input to its 1-state. *Note.* – The use of the dynamic input symbol (12-07-07) at the input is optional (for example of use see symbol 12-45-01).
12-44-02		Monostable, non retriggerable (during the output pulse), general symbol The output changes to its 1-state only when the input changes to its 1-state. The output returns to its 0-state after a period of time which is characteristic of the particular device, regardless of any changes of the input variable during this period. *Note.* – The use of the dynamic input symbol (symbol 12-07-07) at the input is optional (for example of use see symbol 12-45-02).

SECTION 45 – EXAMPLES OF MONOSTABLE ELEMENTS

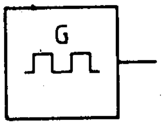
<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>12-45-01</td><td>
</td><td>Monostable, retriggerable
(e.g. part of SN 74LS123)

Function table:

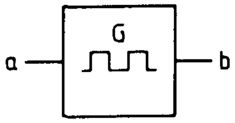
<table>
<tr><th colspan="3">Inputs</th><th colspan="2">Outputs</th></tr>
<tr><th>1</th><th>2</th><th>3</th><th>13</th><th>4</th></tr>
<tr><td>–</td><td>–</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>H</td><td>–</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>–</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>ʃ</td><td>H</td><td>⎍</td><td>⊔</td></tr>
<tr><td>ʅ</td><td>H</td><td>H</td><td>⎍</td><td>⊔</td></tr>
<tr><td>L</td><td>H</td><td>ʃ</td><td>⎍</td><td>⊔</td></tr>
</table>

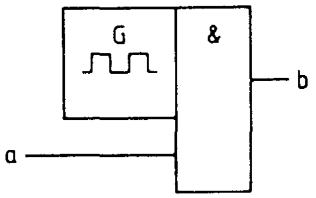
Note. – The second and third line of the function table each indicate the logic levels the outputs will take on after the completion of any output pulse started before the relevant input took on its indicated level.</td></tr>
<tr><td>12-45-02</td><td>
</td><td>Monostable, non-retriggerable
(e.g. part of SN 74221)</td></tr>
</table>

SECTION 46 – ASTABLE ELEMENTS

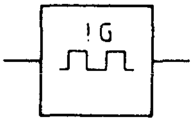
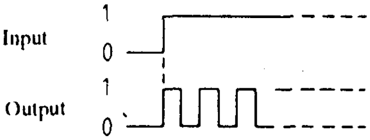
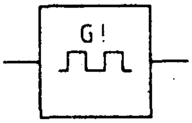
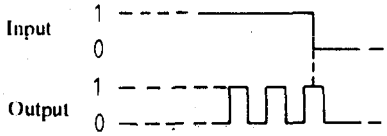
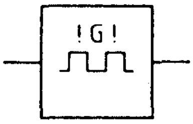
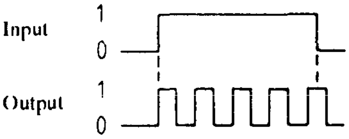
<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>12-46-01</td><td>
</td><td>Astable element, general symbol

Signal generator producing an alternating sequence of zeroes and ones.

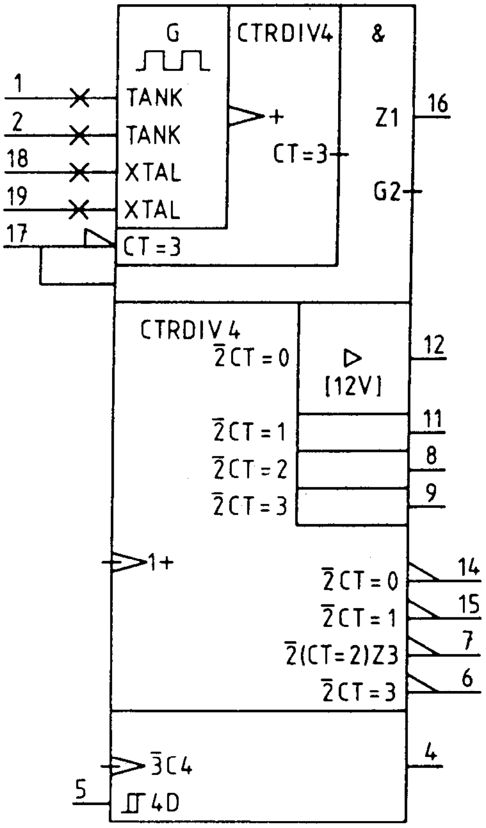
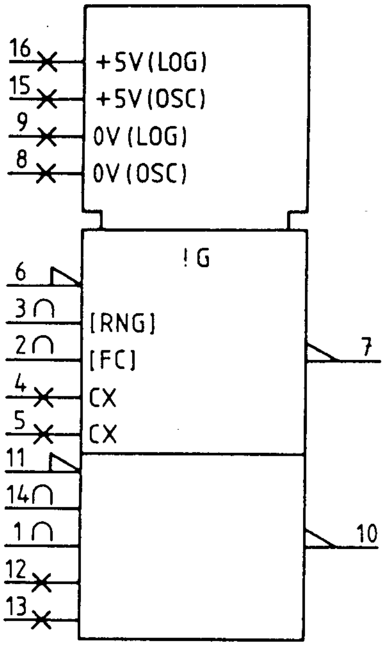
Note. – In this symbol, the G is the qualifying symbol for a generator. If the waveform is evident, this symbol may be shown without the additional symbol ⎍⎍ .</td></tr>
<tr><td>12-46-02</td><td>
</td><td>Controlled astable element, general symbol

Explanatory diagram:


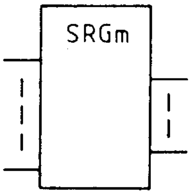
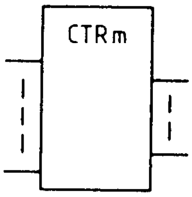
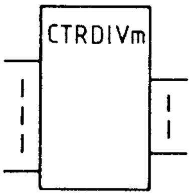
The note with symbol 12-46-01 applies.</td></tr>
</table>

No.	Symbol	Description
12-46-03		**Astable element, synchronously starting, general symbol** The output starts with a complete pulse at the instant at which the input takes on its internal 1-state.  The note with symbol 12-46-01 applies.
12-46-04		Astable element stopping after completing the last pulse, general symbol When the input returns to its internal 0-state, the output remains at its internal 0-state or completes its final pulse.  The note with symbol 12-46-01 applies.
12-46-05		Astable element, synchronously starting, stopping after completing the last pulse, general symbol  The note with symbol 12-46-01 applies.

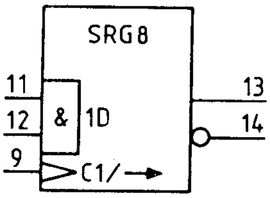
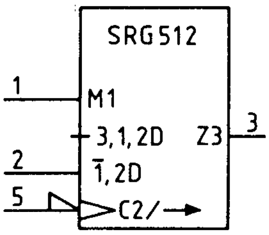
SECTION 47 – EXAMPLES OF ASTABLE ELEMENTS

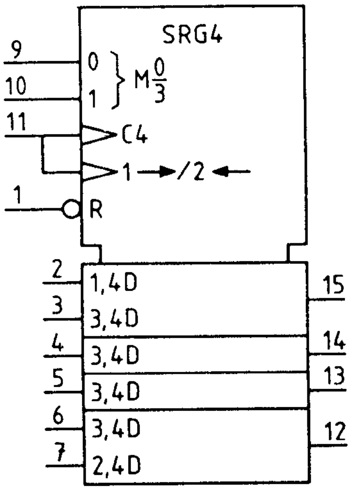
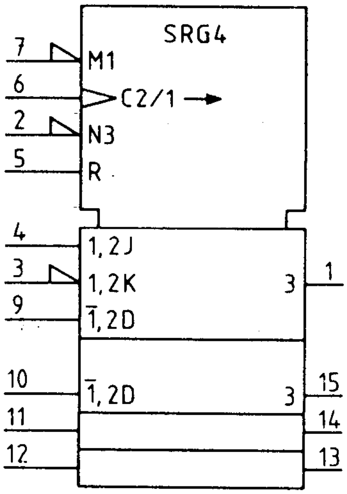
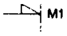
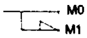
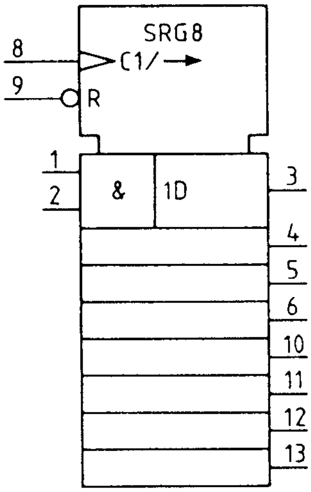
No.	Symbol	Description
12-47-01	 G CTRDIV4 & 1 2 18 19 17 TANK TANK XTAL XTAL CT=3 + CT=3 Z1 16 G2 CTRDIV4 $\overline{2}$CT=0 [12V] 12 $\overline{2}$CT=1 11 $\overline{2}$CT=2 8 $\overline{2}$CT=3 9 1+ $\overline{2}$CT=0 14 $\overline{2}$CT=1 15 $\overline{2}$(CT=2)Z3 7 $\overline{2}$CT=3 6 $\overline{3}$C4 4 5 4D	Clock generator/driver, four-phase (e. g. TIM 9904, formerly SN 74LS362) *Note.* – For the use of CTRDIV4 see symbol 12-48-03.
12-47-02	 16 +5V(LOG) 15 +5V(OSC) 9 0V(LOG) 8 0V(OSC) !G 6 3 [RNG] 2 [FC] 4 CX 5 CX 7 11 14 1 10 12 13	Voltage-controlled oscillator, dual (e.g. SN 74S124) *Note* – If it is not necessary to detail the supply arrangements, the common control block may be omitted.

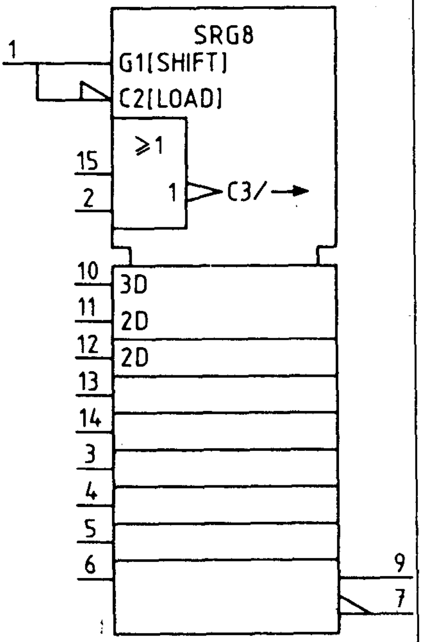
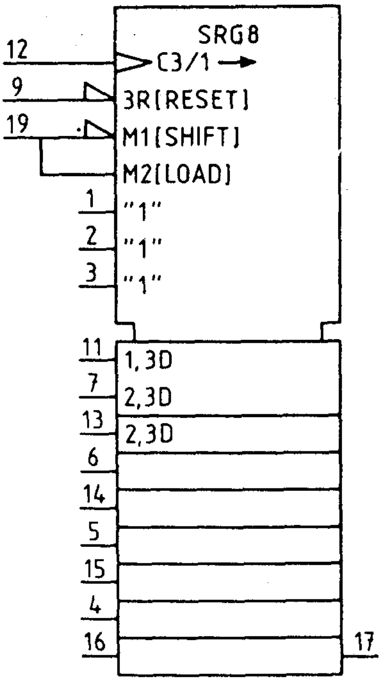
SECTION 48 – SHIFT REGISTERS AND COUNTERS

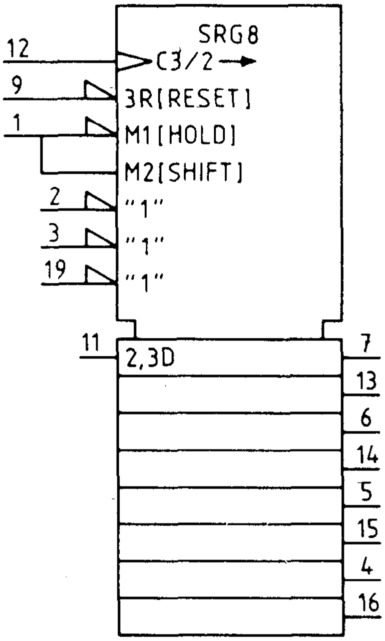
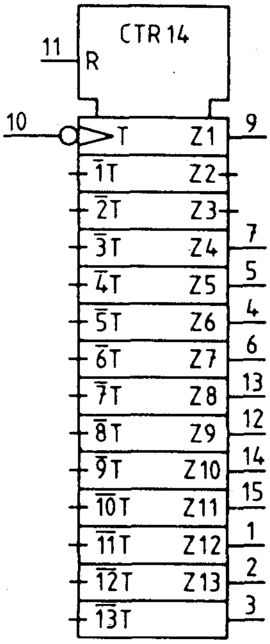
No.	Symbol	Description
12-48-01		Shift register, general symbol *Note.* – The m must be replaced by the number of stages.
12-48-02		Counter with cycle length 2 to the power m (counter modulo 2 to the power m), general symbol *Note.* – m should be replaced by the actual value.
12-48-03		Counter with cycle length m (counter modulo m), general symbol The note with symbol 12-48-02 applies. *Note.* – In an array of elements having different cycle lengths, that applying to each should be indicated by DIVm in each element. In such a case, the letters CTR need only be shown in the common control block (for example of application see symbol 12-49-12).

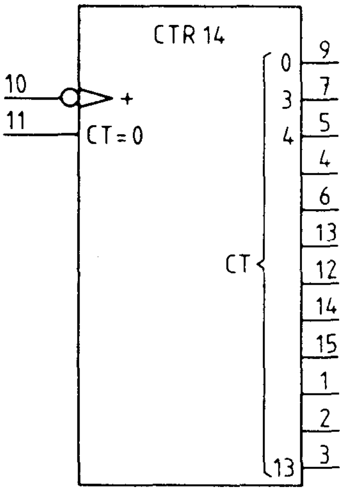
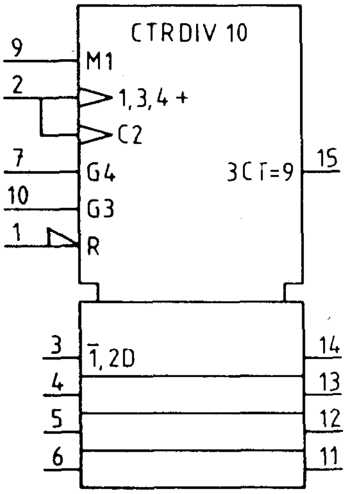
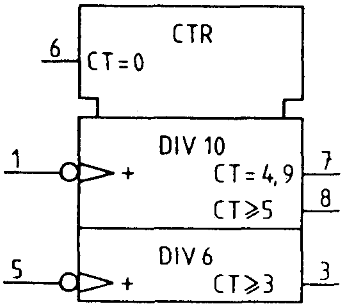
SECTION 49 – EXAMPLES OF SHIFT REGISTERS AND COUNTERS

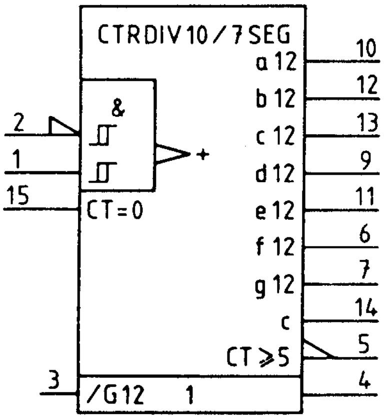
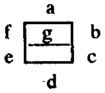
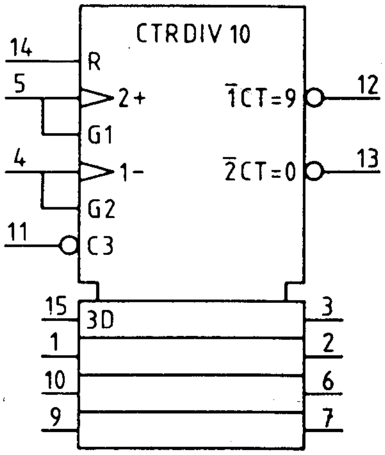
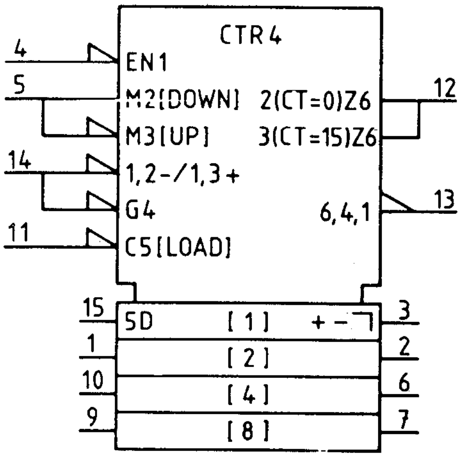
No.	Symbol	Description
12-49-01		Shift register, 8-bit, with serial input and complementary serial output (e.g. part of SN 7491)
12-49-02	 SRG512 1 M1 3,1,2D Z3 3 2 1̄,2D 5 C2/→	Shift register, 512-bit, static (e.g. MM 4057)

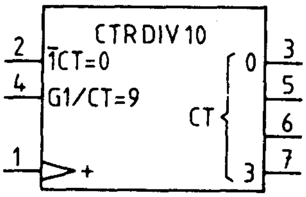
No.	Symbol	Description
12-49-03	 SRG4 9 10 11 1 0 1 M 0/3 C4 1→/2← R 2 3 4 5 6 7 1,4D 3,4D 3,4D 3,4D 3,4D 2,4D 15 14 13 12	Shift register, 4-bit, bidirectional universal (e.g. SN 74LS194)
12-49-04	 SRG4 7 6 2 5 M1 C2/1→ N3 R 4 3 9 1,2J 1,2K 1̄,2D 3 1 10 11 12 1̄,2D 3 15 14 13	Shift register, 4-bit, parallel in/parallel out (e. g. CD 4035A) *Note.* – The use of the bar can be avoided by replacing  by  and 1̄ by 0.
12-49-05	 SRG8 8 9 C1/→ R 1 2 & 1D 3 4 5 6 10 11 12 13	Shift register, 8-bit, with parallel outputs (e.g. SN 74164)

No.	Symbol	Description
12-49-06	 SRG8 1 G1[SHIFT] C2[LOAD] ≥1 15 2 1 C3/→ 10 3D 11 2D 12 2D 13 14 3 4 5 6 9 7	Shift register with parallel load, 8-bit (e. g. SN 74165)
12-49-07	 SRG8 12 C3/1→ 9 3R[RESET] 19 M1[SHIFT] M2[LOAD] 1 "1" 2 "1" 3 "1" 11 1,3D 7 2,3D 13 2,3D 6 14 5 15 4 16 17	Register, universal shift/storage, 8-bit (e.g. SN 74LS323) for which only the reset, shift and parallel load modes are shown. *Note.* – This symbol illustrates how an incompletely utilized device may be represented by a symbol suited to the application. For this purpose use is made of the fixed-mode input, symbol 12- 09-49.

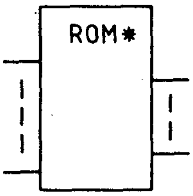
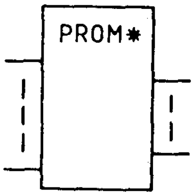
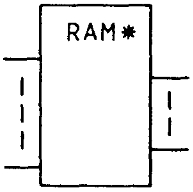
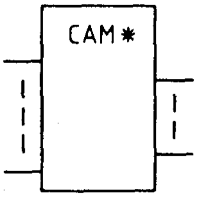
No.	Symbol	Description
12-49-08	 SRG8 C3/2→ 3R[RESET] M1[HOLD] M2[SHIFT] "1" "1" "1" 2,3D 12 9 1 2 3 19 11 7 13 6 14 5 15 4 16	Register, universal shift/storage, 8-bit (e. g. SN 74LS323) for which only the reset, hold and shift modes are shown The note with symbol 12-49-07 applies.
12-49-09	 CTR14 R T 1T 2T 3T 4T 5T 6T 7T 8T 9T 10T 11T 12T 13T Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8 Z9 Z10 Z11 Z12 Z13 11 10 9 7 5 4 6 13 12 14 15 1 2 3	Binary ripple counter, 14-stage (e.g. CD 4020) *Note.* – If it is not necessary to indicate the ripple effect, symbol 12-49-10 may be used.

No.	Symbol	Description
12-49-10	 CTR 14 10 11 + CT=0 0 3 4 CT 13 9 7 5 4 6 13 12 14 15 1 2 3	Binary counter, 14-stage (e.g. CD 4020) *Note.* – If it is necessary to indicate the ripple effect, symbol 12-49-09 shall be used.
12-49-11	 CTRDIV 10 9 M1 2 1,3,4 + C2 7 G4 10 G3 1 R 3CT=9 15 3 1̄,2D 4 5 6 14 13 12 11	Counters, synchronous, decade, with parallel load (e.g. SN 74LS160)
12-49-12	 CTR 6 CT=0 DIV 10 1 + CT=4,9 CT≥5 7 8 DIV 6 5 + CT≥3 3	Counter, one dividing by 5 and 10 and the other by 6 (e. g. SN 49711)

No.	Symbol	Description
12-49-13	 CTRDIV10/7SEG & 2 1 15 CT=0 + a12 b12 c12 d12 e12 f12 g12 c CT≥5 10 12 13 9 11 6 7 14 5 4 3 /G12 1	Decade counter/divider with decoded 7-segment display outputs (e.g. CD 4026) Segment identification: 
12-49-14	 CTRDIV10 14 R 5 2+ G1 4 1− G2 11 C3 1CT=9 12 2CT=0 13 15 3D 1 10 9 3 2 6 7	Counter, decade, synchronous up/down (e.g. SN 74192)
12-49-15	 CTR4 4 EN1 5 M2[DOWN] 2(CT=0)Z6 12 M3[UP] 3(CT=15)Z6 14 1,2−/1,3+ G4 6,4,1 13 11 C5[LOAD] 15 5D [1] +− 1 [2] 10 [4] 9 [8] 3 2 6 7	Binary counter, 4-bit, synchronous up/down, shown with supplementary clarifying information in the array (e.g. SN 74191)

No.	Symbol	Description
12-49-16	 CTRDIV10 1CT=0 G1/CT=9 CT 0 3 + 2 4 1 3 5 6 7	Counter, decade (e.g. part of SN 74490)

SECTION 50 – MEMORIES

No.	Symbol	Description
12-50-01		Read-only memory, general symbol *Note.* – The asterisk must be replaced by an appropriate indication of the number of addresses and bit. In such indications 1k stands for 1024.
12-50-02		Programmable read-only memory, general symbol The note with symbol 12-50-01 applies.
12-50-03		Random-access memory (read/write memory), general symbol. The note with symbol 12-50-01 applies.
12-50-04		Content addressable memory (associative memory), general symbol The note with symbol 12-50-01 applies.